A 0.23 μg Bias Instability and 1.6 μg/Hz^{1/2} Resolution Silicon Oscillating Accelerometer with Build-in Σ-Δ Frequency-to-Digital Converter

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Abstract: This paper presents a silicon oscillating accelerometer (SOA) with CMOS readout circuit. To reduce the bias instability, a PLL is employed to sustain the oscillation instead of the conventional auto-amplitude-control (AAC) circuit. A sigma-delta frequency-to-digital converter (FDC) is built in the PLL to produce the digital output. The MEMS sensor and readout circuit are fabricated in 80 μm SOI and standard 0.35 μm CMOS process, respectively. The SOA achieves 0.23 μg bias instability and 1.6 μg/Hz^{1/2} resolution with ±30 g full-scale, which are equivalent to 4-ppb relative instability and 27-ppb/Hz^{1/2} resolution. In addition, it only consumes 2.7 mW under a 1.5 V supply.

Introduction

Inertial navigation sets a very stringent requirement on long-term stability of the accelerometer, which is characterized by bias-instability. For this requirement, SOA has proven to be a promising candidate compared with the capacitive accelerometer. So far, most of readout circuits in SOAs are realized with AAC technique to stabilize the oscillation. However, due to the amplitude-stiffening (A-S) effect, the flicker noise in AAC circuit appears in the drive signal and deteriorates the bias instability. By employing flicker noise attenuation techniques in AAC, a MEMS SOA with 0.4 μg bias instability and 1.2 μg/Hz^{1/2} resolution with ±20 g full scale was reported recently [1]. Since the flicker noises from AAC circuit in two oscillator channels are uncorrelated, though employing attenuation techniques, the residual noises still deteriorate the bias instability, and are difficult to eliminate. An alternative way to sustain oscillation without using AAC topology was reported in [2]. It can eliminate the noise from AAC circuit, however, it suffers from noise aliasing and the performance is poor.

System Description

This paper demonstrates a SOA with a novel architecture, in which the AAC circuit is completely eliminated without noise aliasing. Fig.1 shows the system block diagram of the proposed SOA. Two oscillator channels are formed with MEMS resonators that are connected to the proof mass. When subject to input acceleration, the two oscillation frequencies change in opposite directions and their difference measures the acceleration. In each oscillator channel, a PLL is employed to track the phase of the front-end TIA’s output (oscillator output) and provide correct phase shift for the drive signal to sustain the oscillation. Meanwhile, the drive signals for both oscillators are correlated, therefore the A-S effect induced flicker frequency noise can be cancelled at the final output (f_1-f_2). Hence the bias instability can be further improved. Furthermore, a third-order Σ-Δ FDC is employed with the phase quantizer embedded in the PLL loop, to digitize the frequency output.

To start the oscillation initially, a start-up circuit is required. At start-up phase, S1 is on and S2 is off. The start-up circuit provides feedback signal with correct phase and amplitude to drive the MEMS resonator and start oscillation. Meanwhile, the PLL will lock to the phase of the front-end output. When oscillation is stabilized, the oscillation detector turns S1 off and S2 on, and the system enters operation phase, in which the feedback loop via PLL takes over to sustain the oscillation, and the start-up circuit will be turned off to save power. The oscillation detector has hysteresis characteristics to prevent the start-up circuit from switching back.

PLL Phase tracking and FDC

The PLL in Fig.1 is the key building block, it not only tracks the phase to sustain the oscillation, but also performs frequency to digital conversion.

Generally, the sinusoidal oscillation signal from front-end output needs to be shaped to square wave before feeding to the PLL. As the noise from front-end is relatively wide-band, i.e. at least several times higher than the oscillating frequency, the waveform shaping will introduce noise folding and cause high in-band noise. To avoid problem, a PLL with hybrid PFD is proposed to do away with the nonlinear waveform shaping. This PFD consists of an analog multiplier phase detector (PD) and a 3-states PFD with large deadzone. When sine wave applies to the input, the 3-state deadzone PFD detects the frequency difference, and helps the PLL to converge. Once the frequencies are close to each other, the 3-state PFD will be automatically disabled due to its large dead zone and the analog PD will take over, to detect the phase difference between the input sine wave and the feedback signal continuously. With the hybrid PFD, both frequency and phase can be tracked, while the noise folding due to waveform reshaping is avoided. The switchover behavior works under all corners in simulations, as well as in the experiments.

The schematic of proposed hybrid PFD is shown in Fig.2(A). The multiplier is implemented by a trans conductor (Gm) and an switching multiplier, where the Gm converts the input sinusoidal voltage to current and then multiplied with the quantized feedback signal (f_{fb}). Thus, the phase error can be detected. To prevent the flicker noise of Gm cell from contaminating the detected phase error, the V to I conversion is performed in AC domain before the multiplier. And the Gm utilizes an OTA and a capacitive feedback to achieve excellent linearity. A pair of pseudo-resistor is used to set the DC bias of the OTA. The hybrid PFD has a fully differential topology with CMFB, to reject common-mode interference.

To convert the oscillation frequency to digital output, the FDC is implemented by embedding a phase quantizer (Fig.2(B)) in the feedback path of PLL after the divider. In this way, the quantization noise induced by DFF1 will be attenuated by the PLL loop and third-order shaped. Therefore for the same resolution requirement, the clock frequency and
hence the power consumption can be significantly reduced. In addition, due to the fully differential topology of SOA, the requirement of clock reference (common to both channels) is also relaxed.

Fig. 2(C) shows the front-end TIA, which adopts the first stage of the band-pass front-end in [1], to achieve low power.

**Measurement Results**

The MEMS sensor is fabricated in SOI process with 80-μm thickness in a wafer-level vacuum package and sealed in a ceramic package. The intrinsic frequency of each resonator is designed to be 18 kHz, while the scale factor is about 200 Hz/g. The quality factor of resonators is around 15,000.

The start-up behavior has been recorded and plotted in Fig.3, which shows that the system can correctly switch over to PLL tracking mode after initial start-up. The measured performance of the SOA are shown in Fig.4. The MEMS sensor can achieve 50 ppm nonlinearity within ±30 g range through centrifugal test. The static performance of the SOA is evaluated at its analog and digital outputs, respectively. The clock frequency is only 750 kHz. The SOA achieves 0.23 μg bias-instability and 1.6 μg/Hz² resolution, which is equivalent to 4-ppb relative instability and 27-ppb/Hz² resolution if taking full-scale into consideration. At higher frequency, 3rd-order noise shaping can be observed. The SOA, including readout circuit chip, consumes only 2.7 mW under a 1.5 V supply. Fig.5 gives the comparison of this work with state-of-the-art SOA and capacitive accelerometers. The readout circuit is implemented in a standard 0.35 um CMOS process and occupies 10 mm² which is smaller than the MEMS chip. Fig.6 is the chip microphotograph.

**References**
