AN ON-CHIP PHASE COMPENSATION TECHNIQUE IN FRACTIONAL-N FREQUENCY SYNTHESIS

Woogeun Rhee and Akbar Ali
Conexant Systems, Inc.*
Newport Beach, California 92660, USA
*Formerly, Rockwell Semiconductor Systems, Inc.

ABSTRACT

Fractional-N frequency synthesis relaxes the phase-locked loop (PLL) design constraints to achieve a low noise performance while providing the same channel spacing. Inherent spurs generated by this system can be reduced with various techniques. The proposed architecture effectively compensates the periodic phase error in the time domain so that it is useful with widely used charge-pump PLLs. An on-chip tuning by a delay-locked loop (DLL) is also provided to make the system less dependent on the output frequency and process variations without using any external element. Simulation results show that the fractional spurs can be completely removed with charge-pump PLLs when ideal matching is assumed.

1. INTRODUCTION

The performance of a frequency synthesizer used as a local oscillator is important for the overall RF system. Frequency synthesis by utilizing a phase-lock technique has been a natural choice in most low-cost wireless applications to accurately control the output frequency with a fixed reference source. Being a feedback system, the PLL-based frequency synthesizers are bandwidth-sensitive to have the desired performance in terms of the phase noise, the reference spur and the settling time. In the standard frequency synthesizer with an integer divider, the phase comparison frequency that limits the loop bandwidth is the same as the channel spacing. Therefore, there is a fundamental tradeoff between the loop bandwidth and the channel spacing in the standard frequency synthesizers.

2. FRACTIONAL-N FREQUENCY SYNTHESIS

Fractional-N frequency synthesis allows PLL-based synthesizers to have a frequency resolution finer than the reference frequency [1]. Figure 1 shows the block diagram of the fractional-N frequency synthesizer. In fractional-N frequency synthesis, a dual-modulus divider is used and the fractional-N division is obtained by periodically changing the division value from N to N+1. For example, to achieve an N+1/4 division, an N+1 division is done after every three N divisions. The carry of the accumulator is the sequence of {...000100010001...}, where an N+1 division is corresponding to "1". The unique problem of this method is the generation of unwanted spurs in addition to the reference spur, which are caused by the periodic operation of the dual-modulus divider. Fractional-N frequency synthesis is not useful in practical applications unless the fractional spurs are removed. Thus, additional circuitry must be added to suppress those fractional spurs. Various techniques have been proposed and their performances are summarized in the literature [2].

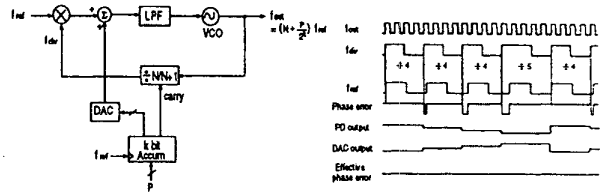

Figure 1. Fractional-N frequency synthesizer (N_{eff}=4+1/4).

2.1. Why fractional-N?

Since the phase-comparison frequency is higher than the frequency resolution in fractional-N frequency synthesis, the loop bandwidth of the PLL is not limited by the frequency resolution as long as the spur cancellation circuit provides an ideal performance. For high-cost frequency synthesizers like HP8662A signal generator, the fractional-N loop is employed as an auxiliary loop in the multi-loop PLL having the bandwidth wider than the frequency step to generate very fine resolution of 0.1Hz. For low-cost and low-power ICs, however, the fractional spur still limits the overall performance and the bandwidth may not be significantly wider than that of the conventional PLL. Even if the bandwidth of the fractional-N synthesizer is as low as that of the integer-N synthesizer, the design tradeoffs in standard frequency synthesizers with an integer divider can be much relaxed with fractional-N technique.

The advantages of using fractional-N technique are summarized as follows. Firstly, the phase noise contribution from the PLL is less when it is referred to the output phase noise. For example, suppose that the output phase noise of -80 dBc/Hz at 1-kHz offset from the carrier is needed to meet the synthesizer specification. When the output frequency of 2 GHz is assumed with the phase-comparison frequency of 200 kHz, the division value is 10,000. If the loop bandwidth is wider than 1 kHz, the PLL circuit noise should be as low as -160 dBc/Hz due to the multiplication factor of 20log(10000). When the fractional-N method is used with a 6-bit accumulator, the phase-comparison frequency is 12.8 MHz with 64-modulo operation. Then, the required phase noise contribution from the PLL circuits becomes only -124 dBc/Hz which can be easily met in CMOS with low-power consumption. Secondly, the reference spur is less sensitive to the leakage current and any non-ideal effects of the charge pump due to high comparison frequency. With the 64-modulo fractional-N technique, the leakage current as high as 10 nA and the 10% mismatch of the charge pump do not affect the spur performance significantly while they are critical in the integer-N frequency synthesizers

0-7803-5471-0/99/$10.00©1999 IEEE

[3]. Different from the reference spur, the fractional spur is considered a systematic error which is predictable with the knowledge of the loop parameters. If the amount of the spur suppression from the spur cancellation circuit is known, the spur can be predicted precisely. Thirdly, the fractional-N technique provides the opportunity of using dynamic bandwidth method more efficiently [4],[5]. Some applications employ the fractional-N technique not to achieve faster settling time but to relax the PLL requirements in terms of the noise contribution and the reference spur. They obtain faster settling time by using the dynamic bandwidth combined with the fractional-N method. By dynamic bandwidth, we mean that the loop bandwidth is set to be wider than the desired one when the PLL is out-of-lock-in range to obtain the faster settling time during the transient mode. However, the loop bandwidth even in the transient mode may not be more than 1/10 of the reference frequency due to stability concerns. With high comparison frequency, the loop bandwidth in the transient mode can be set high without causing any overshoot problem.

2.2. Spur Reduction Techniques

As shown in Fig. 1, the phase error cancellation using a digital-to-analogue converter (DAC) is the traditional method to reduce the periodic tones. The value of the accumulator carries the information of the spurious beat tone, which allows the DAC to predict the phase error for cancellation. This approach is effective when a sample-and-hold (S/H) phase detector is used. For the S/H phase detector, the DAC needs to match only the dc voltage during one reference clock period. Another method is using an oversampling Δ–Σ modulator to interpolate fractional frequency with a coarse integer divider [6]. Since 2nd- or high-order Δ–Σ modulators do not generate fixed tones for dc inputs theoretically, they effectively shape the phase noise without causing any spur. This method is similar to the random jittering method [7], but it does not generate a $1/f^2$ phase noise due to the noise shaping property of the Δ–Σ modulator. Compared to the DAC cancellation method, arbitrarily fine frequency can be generated with digital modulation and it is less sensitive to analog mismatches. However, this technique suffers from hardware complexity and relatively high power consumption. Even though there are more techniques in addition to the DAC cancellation and the Δ–Σ modulation, these two are mostly used as practical solutions. In most commercial RF applications, the low-noise external voltage-controlled oscillator (VCO) is available and the settling time requirement is not so tight for the standard integer-N frequency synthesizers. In other words, the wideband PLL is not necessary in most cases. Therefore, the fractional-N architecture is taken mainly to relax the noise contribution and the reference spur requirement of the synthesizer. With this situation, the conventional digiphase technique with small number of modulo is rather useful to implement low-cost and low-power frequency synthesizers. In this work, the conventional approach is focused and the improved architecture is presented.

3. PROPOSED ARCHITECTURE

Figure 2 shows the proposed architecture with an on-chip tuning technique [8]. Different from the DAC cancellation method, the phase compensation is done before the P/FD. The on-chip tuning circuit corrects the different amount of phase interpolation as the output

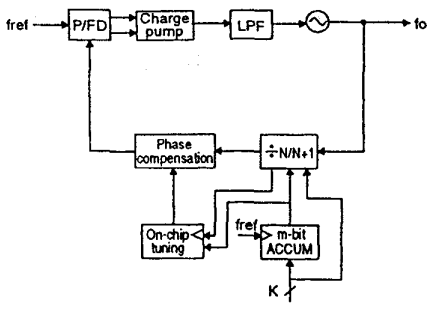

Figure 2. Proposed architecture.

frequency varies. The detailed diagram regarding the phase interpolation and the on-chip tuning is shown in Fig. 3. In this diagram, the modulo-4 operation is assumed with a 2-bit accumulator. The output period, T_{vco}, with the reference frequency, T_{ref}, is given by

$$T_{ref} = T_{vco} \cdot \left(N + \frac{1}{4}\right) \tag{1}$$

The instantaneous timing error due to the divide-by-N is determined by

$$\Delta t_N = T_{ref} - N \cdot T_{vco} = T_{ref}\left(1 - \frac{N}{N + \frac{1}{4}}\right) = \frac{T_{vco}}{4} \tag{2}$$

Similarly, the instantaneous timing error due to the divide-by-N+1 is given by

$$\Delta t_{N+1} = T_{ref} - (N+1) \cdot T_{vco} = T_{ref}\left(1 - \frac{N+1}{N + \frac{1}{4}}\right) = -\frac{3}{4}T_{vco} \tag{3}$$

Therefore, the timing error sequence is {..., $+T_{vco}/4$, $+T_{vco}/4$, $+T_{vco}/4$, $-3T_{vco}/4$, ...} for the division of N+1/4. Similarly, the timing error sequences are {..., $+T_{vco}/2$, $-T_{vco}/2$, ...} and {..., $+3T_{vco}/4$, $+3T_{vco}/4$, $+3T_{vco}/4$, $-T_{vco}/4$, ...} for the division of N+1/2 and N+3/4, respectively. Since the timing error sequence can be predicted from the input of the accumulator, the timing correction is possible if the phase is added with the opposite direction of the timing error sequence. Figure 3 shows this mechanism and the timing diagram is given. By selecting the phase edge periodically from the outputs of the interpolator, from ϕ_1 to ϕ_4, the selected clock will be phase-locked without generating any instantaneous phase error.

The fixed delay element does not offer enough cancellation since the timing error, Δt_N and Δt_{N+1}, depends on the output frequency. As shown in Fig. 3, the delay-locked loop (DLL) is employed to adjust the delay depending on the output frequency as an on-chip tuning solution. It also provides the delay which is less sensitive to process and temperature variations as being referenced to the output frequency. The bandwidth of the DLL should be much wider than that of the PLL so that the settling behavior of the PLL is not corrupted by the DLL. The wideband DLL also makes the on-chip loop filter pos-

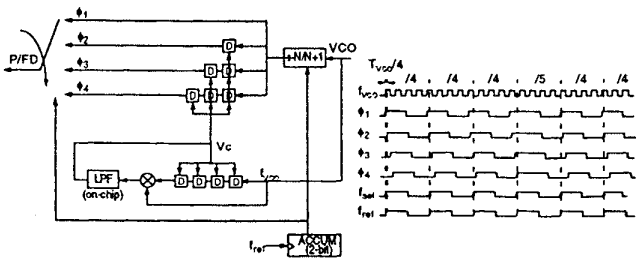

Figure 3. Phase compensation with on-chip tuning (modulo=4).

sible with small area.

Since the input frequency of the DLL is same as the VCO frequency, it is difficult to implement such a high-speed loop with low power consumption. Figure 4(a) shows the improved structure to reduce the input frequency of the DLL. By employing the phase-interpolated frequency divider that consists of two divide-by-2 circuits and phase interpolation block [9], the divide-by-4 output from the VCO is available even with dual-modulus divider. Obviously, this idea can be extended to the divide-by-8, the divide-by-16, and so on. The 16 delay elements give the delay of 4 times the period of the VCO, $4T_{VCO}$, so that each delay cell maintains $T_{VCO}/4$ delay. When the divide-by-16 circuit is used with modulo-8 operation, the number of delay elements would be 128 which is quite a lot to implement. Figure 4(b) shows another improvement to reduce the number of delay cells. Since the multi-phase clock is available from the mentioned interpolated frequency divider, the quadrature outputs may be judiciously taken to reduce the number of delay cells in the DLL when the P/FD is used. Since the DLL does not necessarily needs the P/FD, the different phase must be chosen for the different types of the phase detector. For example, when the flip-flop is used as a phase detector, ϕ_0 and ϕ_{270} should be used instead of ϕ_0 and ϕ_{90}. When the multiplier or the exclusive-or gate are used, ϕ_0 and ϕ_{180} are needed. This improvement takes a risk of degrading the tuning range of the voltage-controlled delay cells and the optimal number of delay cells should be determined with the tuning range issue. Note that the delay cell in the interpolation block is also reduced in Fig. 4(b).

4. COMPARISON WITH EXISTING ARTS

The proposed architecture provides the system solution to remove the periodic tones completely for the charge-pump PLL. Since the P/FD and the charge pump generates the phase error by the pulse-width modulation, the fixed tones cannot be removed by using DAC cancellation method. One approach is to use the programmable charge pump which adds the offset current periodically corresponding to the accumulator output [5]. By compensating the charge pump current, the amount of charge dumped into the loop filter can be same in each cycle. This method is to compensate the area of the pulse by changing the amplitude for different pulse widths. However, the area compensation does not significantly reduce the periodic tones. Another disadvantage of this method is the wide spread of the charge pump current. The ratio of the required offset current to the nominal charge pump current is usually less than 0.1%. For example, a few nA current

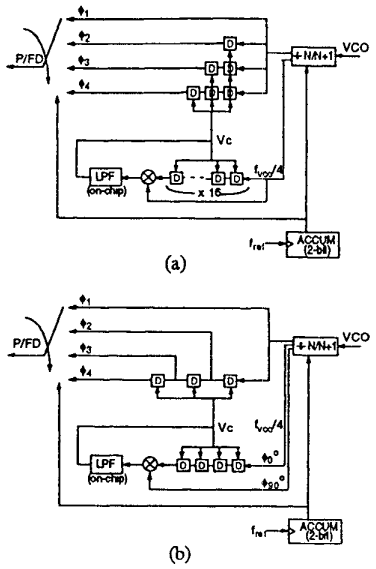

Figure 4. Improved structure : (a) for lower input frequency of DLL, and (b) for reduced number of delay cells.

needs to be added to the 100-μA charge pump current and any mismatch will degrade the performance. Practically, the external resistor is required to have the accurate current value for the compensation. Even when there is no mismatch at all, the spur cannot be completely removed as mentioned above. The proposed technique is superior to the previous one since the spur can be removed as long as the analog matching is perfect. With on-chip tuning, the technique does not require any external resistor and the amount of the delay is constantly changing as the output frequency varies to get the best performance. Compared to the phase-interpolated fractional-N method [10], this architecture does not need multi-phase VCOs like ring-oscillators which are not usually available in RF applications. Since the phase selection is done at baseband, the power consumption is negligible while the phase-interpolation method still needs fast rising edge of the clock to swallow the sub-cycle of the VCO. The proposed technique is useful when the tradeoff in the PLL design needs to be relaxed. Even though Δ–Σ modulated synthesizer provides general solution as a fractional-N frequency synthesizer, the hardware complexity and relatively high power consumption make the proposed architecture more favorable as a practical solution.

5. SIMULATION RESULTS

Behavior simulations were done to verify the system. To reduce the simulation time, a 2nd-order wideband PLL was considered with the division value of 4+1/4 using a 2-bit accumulator. Figure 5(a) shows the output spectrum of the PLL and the control voltage of the VCO. The control voltage at the capacitor of the loop filter is taken to see the averaged waveform. The loop bandwidth is about 20 kHz with 800-kHz reference frequency. The output frequency is 3.4 MHz with the division value of 4.25. As shown in Fig. 5(a), the fractional spur at 200-kHz offset from the carrier without using any cancellation

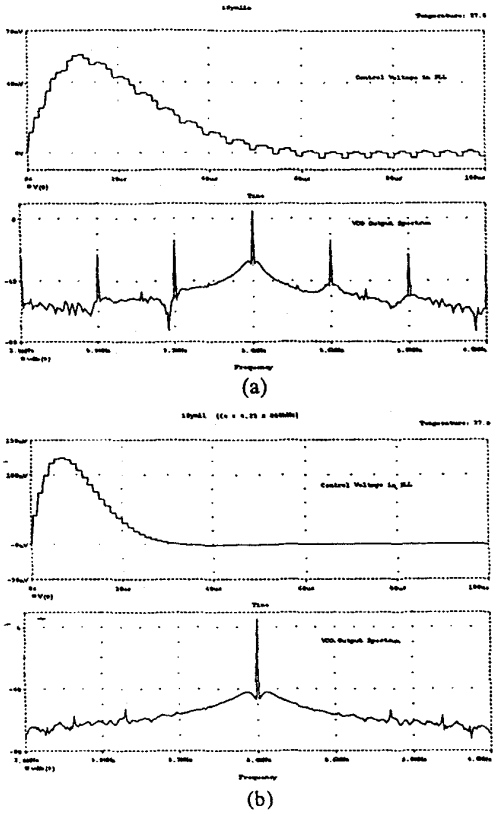

Figure 5. Closed-loop behavior simulation with division of 4+1/4 : (a) without using any cancellation scheme, and (b) with proposed technique.

method is almost -18 dBc. The control voltage clearly shows the fixed tones and the waveform looks different from the one shown in Fig. 1 due to the wide bandwidth. When the proposed method is employed, no spur is observed in the simulation even with 40-kHz loop bandwidth as shown in Fig. 5(b). The waveform of the control voltage does not show any periodic tones. However, the simulation assumes the ideal condition with perfect matching in the interpolation circuits. The simulation with 10% mismatch in the delay elements was also done and the spur was about -40 dBc. That is, the delay mismatch as high as 10% gives only 20 dB suppression limiting the performance. Figure 6 shows the simulation result that includes the on-chip tuning by the DLL instead of using ideal phase-interpolator. In this simulation, the reference frequency is 78 MHz with the division value of 8+1/4, resulting in the output frequency of 643.5 MHz. Each delay element is tuned to have the delay of about 388 psec which is one-forth of the output period. The 3rd-order PLL is taken with 2-MHz loop bandwidth. The waveform, 93, is the reference clock and the waveforms, 930, 931, 932 and 933 are interpolated outputs. The waveform, 94, is the output after the phase compensation with gate pulses, from 9k0 to 9k3, and it is phase locked with the reference clock. The loop bandwidth of the DLL is about 10 MHz which is 5 times higher than the PLL bandwidth.

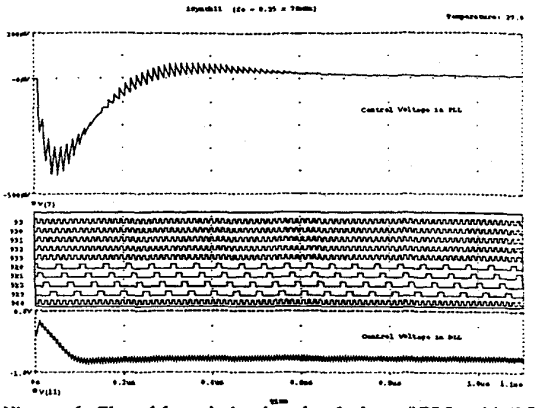

Figure 6. Closed-loop behavior simulation of PLL with DLL.

6. CONCLUSION

A spur reduction technique in fractional-N frequency synthesis with on-chip tuning has been presented. Since the phase compensation is done in the time domain by interpolating the phase, the proposed architecture provides superior performance over the DAC cancellation method when combined with the P/FD and the charge pump. The on-chip tuning scheme by utilizing the DLL removes the fractional spur completely independent of the output frequency and of the process variations when the ideal matching is assumed.

7. REFERENCES

[1] G. C. Gillette, "The Digiphase Synthesizer," *Proc. 23rd Annual Frequency Control Symposium.*, 1969.

[2] D. G. Wilson, W. Rhee, and B. S. Song, "Low Power RF Receiver Front Ends and Frequency Synthesizers for Wireless," *IEEE ISCAS, Tutorial Workshop*, 1996.

[3] W. Rhee, "Design of High-Performance CMOS Charge Pumps in Phase-Locked Loops," *IEEE Proceedings of ISCAS*. Jun. 1999.

[4] D. Byrd and C. Davis, "A Fast Locking Scheme for PLL Frequency Synthesizers," *Application Note*, National Semiconductor Corporation, Jul. 1995.

[5] W. Djen, "SA8025 Fractional-N Synthesizer for 2GHz Band Applications," *Application Note*, Philips Semiconductors, Sep. 1994.

[6] B. Miller and R. Conley, "A Multiple Modulator Fractional Divider," *Proc. 44th Annual Frequency Control Symposium.*, 1990.

[7] V. Reinhardt and I. Shahriary, "Spurless Fractional Divider Direct Digital Synthesizer and Method," *U.S. Patent 4,815,018*, Mar. 21, 1989.

[8] W. Rhee, "Phase-Interpolated Fractional-N Frequency Synthesizer with On-Chip Tuning," *U.S. Patent pending.*

[9] J. Craninckx and M. Steyaert, "A 1.75-GHz/3-V Dual Modulus Divide-by-128/129 Prescaler in 0.7 μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 890-897, Jul. 1996.

[10] T. Weigandt and S. Mehta, "A Phase Interpolation Technique for Fractional-N Frequency Synthesis," U. C. Berkeley's RF Integrated Circuit Design Group: http://kabuki.eecs.berkeley.edu/rf/.