Signal and Noise Properties of Gallium Arsenide
Microwave Field-Effect Transistors

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I. INTRODUCTION

High frequency gallium arsenide field-effect transistors (GaAs FETs) have demonstrated remarkably low noise figures and high power gains at microwave frequencies. Consequently they are excellent candidates for low-noise amplifiers and receivers for communications and radar applications. For example, single stage GaAs FET amplifiers have exhibited in the laboratory noise figures below 4 dB and gains in excess of 10 dB at 10 GHz (Liechti et al., 1972; Baechtold et al., 1973).

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The basic principle of operation of the field-effect transistor was first described by Shockley (1952). He proposed the device as a new semiconductor amplifier based on majority carrier flow, rather than on bipolar flow as for the conventional transistor. As conceived by Shockley the FET is in essence a semiconductive device containing a current path, whose conductance is modulated by the application of an electric field transverse to the direction of current conduction.

Figure 1 illustrates the model of the junction field-effect transistor (JFET) proposed by Shockley. Shown is a slab of n-type semiconductor with an ohmic contact on either end, and two p-type junction contacts on opposite sides. When a positive potential $V_{dd}$ is applied between the two ohmic contacts as shown, electrons flow from the left contact, called the source electrode, to the right contact, the drain electrode. If in addition a bias voltage $V_{gs}$, negative with respect to the source, is applied to the remaining control or gate electrodes (assumed connected together), the $p-n$ junctions become reverse biased. The resulting transverse field depletes carriers from the vicinity of the junction, forming a depletion or space-charge region. As a result, the cross section of the current path, called the channel, becomes...
constricted. Since the extent of the depletion region can be controlled by the gate bias, the drain current will be modulated by the bias voltage. In principle, the modulation of the current path requires negligible power because the junction is reverse biased; therefore, the FET is an active device, capable of power gain.

The conductance of the channel under the gate can also be controlled by varying the concentration of carriers, rather than the cross section. This is the principle of the metal-oxide-semiconductor FET (MOSFET). In this device, the gate junction is replaced by a metallized oxide layer over the semiconductor. MOSFETs so far have not proved suitable for microwave applications and will not be considered here.

Junction FETs may use either a $p-n$ junction for the gate electrode, as assumed by Shockley, or a Schottky barrier junction as proposed by Mead (1966). Of these two types, the Schottky barrier field-effect transistor (SBFET) has exhibited superior microwave properties, especially higher isolation between drain and gate electrodes because of the reduced electrostatic coupling. At present all GaAs FETs are Schottky barrier devices. Although silicon can also be used for microwave SBFETs, because of the higher electron mobility and saturated velocity of GaAs, GaAs FETs can operate at higher microwave frequencies. We shall treat exclusively GaAs SBFETs in our analysis. With changes in some material parameters, the treatment will hold also for silicon devices. The analysis, in principle, also applies to $p-n$ junction structures.

Microwave SBFETs are fabricated by the planar process on a thin conducting GaAs epitaxial layer which has been deposited on a semi-insulating GaAs substrate. The Schottky barrier gate electrode is formed by deposition of a metal, such as gold, on the epitaxial layer.

The operation of a JFET is reminiscent of a vacuum tube wherein the source, gate, and drain electrodes are analogous to the cathode, grid, and plate electrodes, respectively. Indeed, the drain current–voltage characteristics of a JFET based on Shockley's model and illustrated in Fig. 2 look very much like the pentode characteristics of a vacuum tube. For operation below the "knee" of the curves, the depletion region of the gate does not extend across the channel. The region above the knee, in the current "saturation" regime, corresponds to "pinch off" of the channel, that is when the two depletion regions in Fig. 1 have merged into one. Although in principle no carriers are present in the depleted channel, carrier flow is assumed to exist in an infinitesimal sheet.

Basic to Shockley's treatment of the FET is his assumption that the field distribution between the gates can be treated as a superposition of two one-dimensional fields, the longitudinal field, corresponding to charge flow between the ohmic contacts, and the transverse field, corresponding to
FIG. 2. Drain-current-voltage characteristic of Shockley’s FET model. The gate and drain bias potentials are expressed in terms of the pinch-off voltage $W_{oo}$.

charge depletion in the channel. This allows a full analytic treatment of the FET. An assumption underlying this field decomposition is that the channel cross section must vary "slowly" as one moves from the source to the drain, the so-called gradual channel approximation (GCA). The implication of this approximation is that the channel gate length $L$ must be approximately three or more times the channel thickness dimension $a$.

Shockley applied his gradual channel approximation only for bias operating conditions below the knee of the drain current characteristic, that is below the pinch-off point, and assumed that beyond pinch off, the current saturated. He recognized the inadequacy of the GCA beyond saturation because of the strong two-dimensional field distribution near the drain produced by the free charges on that electrode. The strong longitudinal field component generated by these charges violates a basic assumption of the gradual channel approximation.

Before we embark on our exposition, it is appropriate to discuss the various modifications of Shockley’s original theory that have been proposed to account for the current saturation characteristics of the FET. Since an excellent review of this subject has been given in a previous volume of this series by Yang (1972), our discussion shall be brief.

Shockley, in extending his FET analysis beyond pinch off, later divided the channel into two regions: the gradual region from the source electrode to the pinch-off point, and the depleted region from the pinch-off point to the drain electrode. In the depleted region, it was assumed that the electric field and electrostatic potential were determined by the ionized impurity charges
in the depletion region and the free charges on the drain electrode. The joining of the electrostatic potentials for the two regions was postulated to occur at a predetermined position in the channel by a graphical procedure. Later, a more elaborate analytic matching technique was used by Prim and Shockley (1953).

Recently, Wu and Sah (1967) presented a refined matching procedure, in which both potential and electrostatic fields were matched simultaneously. The boundary between the two regions was determined by the matching conditions. Since this boundary position was a function of operating biases, particularly the drain voltage, they showed that current saturation no longer occurred, as in Shockley's model, and that a finite drain resistance could be accounted for by the motion of this boundary with drain voltage. This mechanism for explaining finite drain resistances had been proposed earlier by Reddi and Sah (1965) and by Holstein and Warfield (1965) for MOS FETs, but had not been developed in detail.

Dacey and Ross (1955) were the first to suggest that current saturation in FETs might be attributable to the decrease in mobility at high electric fields. To test this hypothesis, they introduced a field-dependent mobility in Shockley's gradual channel approximation using Shockley's theory (1951) and Ryder and Shockley's (1951) experimental data for germanium. Trofimenkoff (1965) and Tarney (1966) extended Dacey and Ross' treatment by using a better analytic approximation for the experimental mobility data. Zuleeg (1967), carrying this approximation still further, made an analysis based on a three-piece linear approximation of the velocity-field characteristic, which included velocity saturation beyond a certain field. He measured the saturation current for silicon devices as a function of temperature and found the same temperature dependence as that of the limiting drift velocity (1965). This was the first experimental evidence relating current saturation in FETs to velocity-limited flow. Velocity saturation in GaAs FETs appears to have been invoked first by Winteler and Steinemann (1967) to explain current saturation in their experimental devices. Their data suggested a limiting velocity of $10^7$ cm/sec for electrons.

The significance of field-dependent mobility in JFETs with small channel length : thickness ratios was treated in detail first by Hauser (1967) who calculated the shape of the junction depletion region near the ends of the gate using a potential distribution characteristic of semicylindrical electrodes. A significant feature of this model, which differs from previous models, is the absence of complete channel pinch off in the current saturation regime even with no velocity saturation! Inclusion of a limiting carrier velocity greatly decreased the saturation current. The importance of velocity saturation was found to depend on a single parameter, namely $E_s L/W_{00}$, where $E_s$ is a critical field denoting the onset of velocity saturation, $L$ is the gate length,
and $W_{oo}$ the pinch-off voltage. Hauser found that effects of velocity saturation became important when this parameter satisfied the condition $E_c L/W_{oo} < 1/3$. Hauser's treatment, which was based on the idealized Shockley configuration, Fig. 1, was later extended by Mo and Yanai (1970) to short-gate devices having a more practical geometry. Supporting experimental data were presented. Chiu and Ghosh (1971) also treat the shortgate geometry, and, in addition, postulate carrier accumulation in the velocity-saturated region but offer no experimental justification for this assumption. Hofstein and Warfield (1965), however, had shown earlier that the electric fields produced by mobile charges in the velocity-saturated region could be neglected in comparison to the fields originating from free charges on the drain electrode.

The first attempt to analyze velocity saturation effects in GaAs was made by Turner and Wilson (1969). To account for a velocity-saturated electron flow, they postulated a finite channel opening at the drain end of the gate at the onset of drain current saturation. These workers still retained the gradual channel approximation of Shockley throughout the entire channel (with a constant mobility) but imposed the condition that the onset of velocity saturation always began precisely at the drain end of the gate; that is, the critical field for velocity saturation remained "pinned" at this point in the channel. Saturation current levels corresponding to different gate bias voltages could be accommodated by a widening or narrowing of the channel opening at the drain end. Lehovec and Zuleeg (1970) modified this model by replacing the constant mobility with the approximate field-dependent expression proposed earlier by Trofimenkoff (1965). However, although their model assumed complete velocity saturation at the end of the gate, an infinite channel field was necessary at this point at the onset of current saturation, because of the analytic form of the assumed velocity-field expression.

About this same time Grebene and Ghandhi (1969) proposed a two-section model of the FET, based on a two-piece linear approximation of the velocity-field characteristic. As in the Turner–Wilson model the mobility was assumed constant below a critical field $E_c$, and the velocity was assumed constant above this field as shown in Fig. 3. In operation above pinch off the FET was divided into two sections as indicated in Fig. 4. In region I near the source the mobility was assumed constant and Shockley's gradual channel approximation was applicable. In the contiguous region near the drain, region II, the carrier velocity was assumed saturated. In this second region, a conductive channel of finite opening was postulated to account for current continuity and the finite carrier velocity as in the Turner–Wilson model. Unlike the Turner–Wilson model, however, the plane corresponding to the onset of velocity saturation was not "pinned" at the drain end of the gate.
Rather, it was allowed to move into the channel with bias voltage variations as the field distribution demanded, its position being determined by the location at which the longitudinal channel electric field equaled the critical value $E_s$. Because of the automatic adjustment of this plane, the model not only applies to operating conditions below the knee of the $I-V$ characteristic, but also above. Lehovec and Zuleeg (1970) also had suggested this modification of the Turner–Wilson model, but at the outset had assumed that the length of the velocity-saturated region was small compared with the epitaxial channel thickness. Unfortunately, as we shall demonstrate later, this condition is rarely, if ever, fulfilled in microwave devices biased into the current-saturated regime.

The small-signal properties of junction FETs were first analyzed semi-quantitatively by Shockley in his original paper. His analysis, which was applied to germanium and silicon devices, was restricted to the case of constant mobility. Dacey and Ross (1955) extended Shockley's treatment to a field-dependent mobility, more representative of actual devices and compared the predicted performance with Shockley's case. The frequency and power handling capabilities of FETs also were considered.

![Diagram of FET model](image)

**Fig. 4.** Two-section model of the FET used by Grebene and Ghandhi (1969) based on the velocity-field characteristic of Fig. 3.
The first detailed quantitative treatment of the small-signal parameters was made by van der Ziel and Ero (1964). Returning to the constant mobility case of Shockley, they considered the region under the gate as an active, nonuniform transmission line. By obtaining an approximate solution of the resulting nonlinear wave equation in a power series in frequency, accurate quantitative expressions for the intrinsic two-port small-signal parameters were derived which were applicable up to moderately high frequencies. Hauser (1965) also obtained approximate solutions to the transmission line model using an iterative technique. His results, which were in agreement with van der Ziel and Ero, also encompassed the more complicated dual-gate structure.

Somewhat later Geurst (1965) and Paul (1967) obtained an exact solution of the van der Ziel–Ero wave equation in terms of parabolic cylindrical (Weber) functions which extended the applicability of the solutions to still higher frequencies. However, because of the complexity of these functions, a power series expansion in frequency was necessary.

All of the small-signal treatments discussed so far are only valid up to the point at which the channel becomes pinched-off, that is below the "knee" of the $I-V$ characteristic. Unfortunately, FETs are usually operated in the current saturation mode. Therefore, the treatments above postulate that the small-signal parameters evaluated at the pinch-off point (just at the knee) can be applied beyond pinch off with negligible error. This extension appears to be a reasonably good approximation for the input (gate-source) and forward transfer (transconductance) parameters; however, it fails completely to predict a finite output resistance, since the drain current is assumed to remain fixed beyond the knee. As pointed out earlier, this deficiency in the model was removed about this time by others who invoked channel length modulation as the cause of finite drain resistance.

The first treatment of GaAs FETs to include the effects of velocity saturation on the small-signal parameters was made by Turner and Wilson (1969) who attempted to explain the microwave performance of short-gate GaAs FETs using their model described earlier. Based on this same model, the small-signal analysis was developed in a somewhat different way by Wolf (1970) who also derived a small-signal equivalent circuit. Hower and Bechtel (1973), using a modification of Hauser's iterative technique, developed the Turner–Wilson small-signal model in more detail. Taking parasitic contact resistances into account, they compared the predicted dc characteristics and small-signal parameters with experimental results and appeared to obtain reasonable agreement. Turner and Wilson's small-signal model, like van der Ziel's, is valid below the knee of the $I-V$ characteristic only, and must be extrapolated beyond into the saturation regime; therefore it also predicts an infinite drain resistance.
The first comprehensive treatment of noise in FETs was made by van der Ziel in a series of classic papers (1962, 1963a). These analyses, which were based on the small-signal analysis of Shockley's device published later (van der Ziel and Ero, 1964), identified the main source of noise in FETs as thermal noise in the channel. Using a Green's function analysis for the thermal voltage fluctuation distribution along the channel, van der Ziel derived expressions for the drain current and induced gate current noise and also for the correlation between them. A constant mobility was assumed throughout the channel. Shoji (1966) extended van der Ziel's analysis to MOS devices.

Klaassen (1967), using Geurst's (1965) wave analysis for the high frequency parameters of the FET, and van der Ziel's treatment for the thermal noise, extended van der Ziel's results to higher frequencies. He also showed that, unlike van der Ziel's result, the correlation coefficient was complex, rather than imaginary. He attributed this to the influence of the high frequency gate-channel coupling on the noise of the drain current, which van der Ziel neglected. However, it appears that this correction is important only beyond the useful frequency of operation of the FET.

Baechtold, in a series of papers (1971, 1972) was the first to include velocity saturation effects on the noise performance of microwave FETs. Using van der Ziel's analytic treatment of the thermal noise, and the Turner-Wilson model, Baechtold derived noise coefficients as a function of the parameter \( E_s L/W_{00} \) mentioned earlier. These coefficients also were presented in convenient graphical form. Baechtold also included a field-dependent noise temperature based on his experimental data, to account for the "hot" electrons. His analysis, unfortunately, has the same limitations as the Turner-Wilson model, upon which it is based, in that it supposes a velocity saturated region of vanishing extent. Thus it neglects any noise that may be generated by carriers traveling at their limiting velocities.

The assumption that velocity saturation only occurs at the drain edge of the gate, the basis for the Turner-Wilson model, cannot be justified for operating conditions well above the knee of the \( I-V \) characteristic for microwave devices. For example, for a typical microwave device, \( L \approx 1-2 \times 10^{-4} \) cm, and for a drain bias in the current saturated regime \( V_{dd} \approx 2 \) V, the average longitudinal channel field is 10 kV/cm, well above the critical field \( E_s \approx 3 \) kV/cm at which velocity saturation effects first become important. In the analysis to be developed here, we abandon the hypothesis of Turner and Wilson, and instead adopt the two-section model of Grebene and Ghandhi. We show by a correct application of this model that velocity saturation can manifest itself over most of the channel length for GaAs microwave devices having gate lengths of the order of 1 \( \mu \)m.

Our analysis will show that this two-section model not only yields a
good representation of the dc and small-signal characteristics of the GaAs FET, but the noise properties as well. The treatment of the noise for the region below velocity saturation is based on the analyses of van der Ziel, suitably modified to account for the variable boundary position between the two regions. For this region we also adopt Baechtold’s modification for the electron temperature. The noise analysis for the second, or velocity-saturated region, however, is new. It turns out that the noise generated in this region can be very important in microwave devices, and indeed, may dominate the contribution of the unsaturated (van der Ziel) region. Because the correlation between drain and gate noise is also higher, strong noise cancellation occurs, so that the minimum noise figure can still be attractively low and in accordance with experiment.

Our noise treatment of the saturated velocity region in some ways follows a suggestion by Shockley et al. (1966), according to which the high field diffusion constant implies the formation of dipole layers which drift through the high field region toward the drain contact. The high field diffusion constant for GaAs has been measured by Ruch and Kino (1968) and evaluated by Fawcett and Rees (1969). Both the measurements and the calculations show a peak in the parallel diffusion constant near the saturation field, followed by a rapid drop to much lower values. The measurement of the diffusion constant is complicated by trapping effects. We obtain better agreement with noise figure measurements if we use in our expressions values which are consistent with the calculations of Fawcett and Rees. In our analysis, we neglect variations of the diffusion constant with electric field.

We turn now to our analysis of the dc, small-signal, and noise characteristics of GaAs microwave FETs.

II. The Intrinsic FET

A. Introduction

A practical microwave GaAs FET is usually fabricated by deposition or diffusion of source, gate, and drain contacts on the surface of an appropriately doped thin epitaxial n-type layer. This layer, in turn, is grown on a semi-insulating wafer by either a vapor or liquid epitaxial technique. The resistivity of the substrate is of the order of $10^8 \, \Omega\text{-cm}$. On the other hand, the epitaxial layer has a resistivity of about $10^{-2} \, \Omega\text{-cm}$, and a thickness ranging from 0.1 to 0.4 $\mu$m. Thus the substrate for all practical purposes can be considered an insulator insofar as conduction processes are concerned.

A perspective sketch of a practical FET is shown in Fig. 5. This figure, in addition to illustrating the geometrical configuration, also serves to introduce appropriate nomenclature for later reference. Note that all three con-
tacts are in the plane of the epitaxial surface because of the planar technology used. Also observe that a small but finite spacing must separate the gate contact from the source and drain electrodes. For microwave transistors, this spacing is limited to a lower value of approximately 1 μm, dictated by photolithographic restrictions, but is usually several times this value. The gate length $L$, which is one of the crucial dimensions in the FET, is typically of the order of 1–4 μm. Because of the finite separation of the contacts, small parasitic resistances are introduced between the edges of the gate electrode and the source and drain contacts. Added to these resistances are the interfacial resistances under the source and drain electrodes. These parasitic resistances, although important, do not affect the intrinsic operation of the transistor, and can be ignored in a study of the intrinsic characteristics. They affect strongly the noise performance of the FET.

For analytic convenience, we shall consider the idealized model of the FET shown in Fig. 6a. Later we shall show how the analysis of this model can be modified to include the effects of the parasitic resistances introduced by the source and drain contacts. The structure of Fig. 6a can be considered equivalent to one-half of the symmetric FET shown in Fig. 6b which was the configuration conceived by Shockley (1952) and analyzed by van der Ziel (1962). The symmetry plane plays the role of the nonconducting substrate. This structure is a good approximation for the conduction processes of the planar structure of Fig. 5 because of the negligible substrate conductivity; however, it is not an appropriate representation for the capacitance between the source and drain contacts of the planar structure because of the nonzero permittivity of the semi-insulating substrate. For computation of this parasitic capacitance the actual planar geometry will be used.

We shall use the symmetric FET of Fig. 6b for our analysis. It will be mentioned, where necessary, what numerical factors will convert the results to the asymmetric model. Figure 6b defines the pertinent parameters based on the notation of van der Ziel (1962). To avoid unnecessary confusion, and
to facilitate comparison with van der Ziel's results, we shall follow his convention and assume positive carriers, that is a p-type conducting layer. However, since all GaAs transistors are made of n-type material, we shall use in our numerical examples saturated velocities, noise temperatures, mobilities, etc., characteristic of electrons.

Van der Ziel's analysis, as mentioned earlier, is not valid in the current saturation regime, that is when the channel at the drain end is pinched off. The present analysis, in addition to including the presaturation regime, is also valid beyond pinch off; however, we redefine the onset of pinch off to mean the condition at which the maximum longitudinal electric field in the channel first reaches the critical value $E_s$, rather than when full channel depletion occurs, since for a finite $E_s$ full channel depletion cannot take place.

Our assumption of a saturation field above which carriers travel at constant velocity, as illustrated in Fig. 3, disregards a region of negative mobility in the actual velocity-field characteristic. Although this negative mobility is responsible for domain formation and rf oscillations in Gunn diodes, only limited evidence of such instabilities in GaAs FETs has been demonstrated
(Winteler and Steinemann, 1967; Zuleeg, 1968, 1969) and only for doping levels at least an order of magnitude lower than that used for practical FETs. Indeed the computer solutions of Himsworth (1972) point to the possibility of negative resistance effects for lightly doped epi-layers. The apparent minor role played by the negative resistance region in practical short-gate FETs suggests that rf instabilities due to this region, if they exist, occur at frequencies far above the normal frequency regime of microwave FETs, or alternatively, that domain formation is inhibited by the two-dimensional character of the field configuration within the FET (Copeland, 1968) or by the space charge of the carriers at the high injection levels present (Watson, 1969).

B. The dc Conditions

We derive first the dc characteristics of the FET and obtain from these, by a perturbation analysis, relevant small-signal or ac parameters. Let \( x = 0 \) and \( x = L \) represent, respectively, the source and drain reference planes of the channel. The channel of the transistor is separated into two longitudinal sections, Fig. 4, corresponding to the two piecewise linear segments of the assumed velocity-field characteristic of Fig. 3. In region I, \( x < L_1 \), Ohm's law is assumed to hold, \( \mu = \mu_0 \). In region II, \( L_1 < x \leq L \), velocity saturation applies, \( v = v_s \). The boundary between these two regions, \( x = L_1 \), is specified by the condition \( E = E_s \).

The piecewise linear approximation of the velocity-field characteristic necessarily involves compromises in the choice of values used for \( E_s \), \( \mu_0 \), and \( v_s \). We have selected \( \mu_0 = 4500 \text{ cm}^2/\text{V-sec} \) and \( E_s = 2.9 \text{ kV/cm} \) which yield a value for \( v_s = \mu_0 E_s = 1.3 \times 10^7 \text{ cm/sec} \). The choice for \( \mu_0 \) is indeed typical of doping levels used in practical FETs, i.e., \( 10^{16} - 10^{17} \text{ cm}^{-3} \). The value for the saturation field \( E_s \) is somewhat lower than the range \( 3-4 \text{ kV/cm} \) observed and calculated for these doping levels (Ruch and Kino, 1968). Its choice was based on the requirement that the resultant velocity would not exceed the computed range by too great a margin (Ruch and Fawcett, 1970). Despite the compromises, the dc, small-signal, and noise parameters based on them agree extremely well with experiment as will be demonstrated later.

Let the reference or source potential be at ground, and the gate and drain electrode potentials referred to the source be denoted by \( V_{sg} \) and \( V_{sd} \), respectively, as illustrated in Fig. 7a.* Also, let the potential of the channel, at a distance \( x \) from the source be \( V(x) \) and its value at the pinch-off point

* In the idealized model being considered here (no contact resistances) one may assume that the gate and drain channel potentials are equal to the applied bias potentials, i.e. \( V_{sg} = V_{ss} \), \( V_{sd} = V_{dd} \).
$x = L_1$ be denoted by $V_p$, where $V_p = V(L_1)$. It shall be necessary in our analysis to utilize the channel potential referred to the gate electrode. We denote this potential at point $x$, by $W(x)$. (See Fig. 7.) Thus

$$W(x) = V_{sg} + \phi - V(x),$$

where $\phi$ is the "built-in" potential of the gate junction. This barrier potential is typically of the order of 0.8–0.9 V for GaAs Schottky barrier junctions using metals such as gold. The values of $W(x)$ at the source end of the channel, $W_s$, at the drain end, $W_d$, and at the joining point, $W_p$, are given by

$$W_s = V_{sg} + \phi,$$

(2a)

$$W_p = V_{sg} + \phi - V_p,$$

(2b)

$$W_d = V_{sg} + \phi - V_{sd}.$$  

(2c)

Figure 7c illustrates schematically the various potential differences described by these equations.

For a specified source-drain current $I_d$ (with positive carriers), the $E$-field is directed from left to right as indicated in Fig. 7a and the channel potential decreases monotonically to the source-drain bias potential $V_{sd}$ as one moves toward the drain. Therefore, the depletion region between gate and source widens as the drain electrode is approached.

The expressions to be developed later become simplified if we introduce the reduced "potentials"

$$s = (W_s/W_{00})^{1/2}$$

(3a)

$$p = (W_p/W_{00})^{1/2}$$

(3b)

$$d = (W_d/W_{00})^{1/2}$$

(3c)

$$w(x) = [W(x)/W_{00}]^{1/2}$$

(3d)

where $W_{00}$ is the gate-to-channel potential required to deplete the channel of carriers given by

$$W_{00} = (qN/2\kappa\varepsilon_0)a^2.$$  

(4)

Here $q = 1.6 \times 10^{-19}$ C, $N$ is the doping density in the channel in atoms/cm$^3$, $\kappa = 12.5$ is the dielectric constant of GaAs, and $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm is the permittivity of free space. The dimension $a$ is the half

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**Fig. 7.** Cross-sectional diagram of the idealized FET showing various geometrical dimensions and potentials used in the analysis. (a) Bias voltages, channel dimensions, and reduced potentials. In the idealized model shown, parasitic resistances are absent, so that $V_{gs} = V_{ds}$ and $V_{sd} = V_{dd}$. (b) Longitudinal electric field distribution along symmetry plane of channel. (c) Potential distribution along symmetry plane. Also shown is gate bias potential and gate-to-channel potential.
thickness of the semiconductor between the gate electrodes. Note that $W_{oo}$ represents the "pinch-off voltage" for the Shockley model.

The channel-to-gate potential $W(x)$ is obtained by integration of the one-dimensional Poisson equation in the $y$-direction in the depletion region, for a volume charge density $N$. This treatment of the depletion layer potential is justified on the basis that the potential changes along the channel are gradual or, equivalently, that the longitudinal field in the channel is negligible compared to the transverse field in the depletion region (Shockley, 1952). This condition is fulfilled if the channel thickness is much smaller than the total gate length. Since there is no surface charge density at the boundaries of the conducting channel, i.e., the edges of the depletion region, the transverse electric field vanishes there. With this boundary condition, we obtain for $W(x)$ the expression

$$W(x) = W_{oo}[1 - b(x)/a]^2,$$

where $2b(x)$ is the "height" or opening of the channel at point $x$ (Fig. 7a).

The drain current is given in terms of $W(x)$ by Ohm's law,

$$I_d = 2b(x)Z\sigma(\partial W/\partial x),$$

where $\partial W/\partial x = E_x(x)$ is the longitudinal channel field, $Z$ is the width of the gate electrode, Fig. 5, and $\sigma = q\mu_0 N$ is the conductivity of the epitaxial layer. Here $\mu_0$ is the low-field mobility and $N$ is the carrier density.

Integrating Eq. (6) from $x = 0$ to $x = L_1$, using the reduced potential $w(x)$, one obtains

$$I_d = \frac{2g_0 ZW_{oo}}{L_1} \int_{x}^{\rho} (1 - w)w \, dw$$

$$= \frac{g_0 ZW_{oo}}{L_1} f_1(s, p)$$

where

$$f_1(s, p) = p^2 - s^2 - \frac{2}{3}(p^3 - s^3).$$

Here

$$g_0 = 2a\sigma$$

is twice the sheet conductivity of the epitaxial layer of the asymmetric transistor, and $L_1$ the, as yet, undetermined length of region $I$. The form of Eq. (7) was first derived by van der Ziel (1962). (For future reference, whenever $g_0$ appears in an expression, this expression also applies to the asymmetric transistor provided that the factor of 2 in $g_0$ is dropped.)

We may determine $L_1$ by utilizing the current continuity between regions
I and II. In region II the carriers are assumed to travel at their limiting velocity \( v_s \) where

\[
v_s = \mu_0 E_s,
\]

as indicated in Fig. 3. Thus in region II

\[
I_d = g_0 ZE_s(1 - p)
\]

\[
= I_s(1 - p)
\]

where

\[
I_s = g_0 ZE_s
\]

is the maximum possible drain current that could exist if the channel were fully undepleted and the carriers traveled at their saturated velocity. We shall call \( I_s \) the saturation current. It will be used as a convenient normalizing factor for the drain current in the ensuing analysis.

Equating Eqs. (7) and (11), we obtain the relation

\[
E_s L_1 / W_{00} = f_1 / (1 - p)
\]

or, equivalently,

\[
L_1 = L \left[ f_1(s, p) / \xi(1 - p) \right]
\]

(13)

where

\[
\xi = E_s L / W_{00}
\]

is a dimensionless potential parameter which we label the saturation index. The product \( E_s L \) is the voltage drop along the channel which would exist if the longitudinal channel field were constant and equal to \( E_s \). A comparison of \( \xi \) with the normalized source-drain potential \( V_{sd} / W_{00} \) expresses in a quantitative way the importance of velocity saturation. The smaller is \( \xi \), the greater is the role of velocity saturation. For microwave transistors, \( \xi \) is of the order of 0.05–0.40, with the lower values corresponding to the upper end of the microwave range (X band).

Once the reduced potentials \( s \) and \( p \) are known, the length of region I is specified and the current \( I_d \) is determined. Conversely, given the gate bias or (reduced) potential \( s \), and the drain current \( I_d \), \( p \) is determined from Eq. (11) and hence \( L_1 \) is specified from Eq. (13).

Assuming that the channel current is given, one may calculate the channel source-to-drain potential drop by integrating the longitudinal electric field along the channel from \( x = 0 \) to \( x = L \). This integration is done in two parts, from \( x = 0 \) to \( x = L_1 \), and from \( x = L_1 \) to \( x = L \), since the electric field is due to different sources in either region. Integration of the electric field in region I yields the potential drop

\[
V_p = -(W_p - W_s)
\]

\[
= -W_{00}(p^2 - s^2)
\]
as is obvious from an application of Eqs. (1) and (2). In region II the longitudinal electric field is determined entirely by free charges on the drain electrode (if carrier accumulation is neglected) since the carriers travel at their saturation velocity. The potential produced by the free-charges satisfies Laplace's equation. The most general solution of this equation valid for $L_1 \leq x \leq L$ which vanishes at the boundary plane $x = L_1$, and at the gate electrodes $y = \pm a$ is of the form

$$
\Phi(x, y) = \sum_{n=0}^{+\infty} a_n \cos \left[ (2n + 1) \frac{\pi y}{2a} \right] \sinh \left[ (2n + 1) \frac{\pi(x - L_1)}{2a} \right] 
$$

where $n$ is an integer. This form was first suggested by Shockley (1952) and later proposed for the saturated velocity case by Grebene and Ghandhi (1969).

Following Grebene, it is sufficient for our purposes to approximate Eq. (16) by the lowest space harmonic because of the rapidly varying exponentials. Since the longitudinal electric field at $x = L_1$ is assumed to be continuous at the junctions of regions I and II and equal to $E_s$, we obtain for the simplified Laplacian potential

$$
\Phi(x, y) \approx -\frac{2a}{\pi} E_s \cos \frac{\pi y}{2a} \sinh \frac{\pi(x - L_1)}{2a}. 
$$

To this we must add the $x$-independent Poisson potential produced by the ionized impurities of the depletion region. A particular solution of Poisson's equation is obviously the constant potential $-W_{00}(p^2 - s^2)$ within the carrier stream $|y| \leq b_p = a(1 - p)$, and a potential within the depletion region $b_p \leq |y| \leq a$, increasing parabolically toward the gate.

The longitudinal channel drop in region II can be obtained from Eq. (17) by letting $x = L$. Adding this drop to the drop in region I, we obtain for the source-drain potential

$$
V_{sd} = -W_{00} \left[ (p^2 - s^2) + \frac{2}{\pi} \left( \frac{a}{L} \right) \xi \sinh \frac{\pi L_1}{2a} \right]. 
$$

This equation, in conjunction with Eq. (13), forms a pair which allows one to eliminate the unknown $L_1$ and to solve for $p$ given the applied gate and drain potentials $V_{sg}$ and $V_{sd}$. Equation (11a) then yields $I_d$. These highly nonlinear equations in $L_1$ and $p$ are most conveniently solved by computer. Only the solutions satisfying the conditions $0 < s < p \leq 1$ are valid. Alternatively, one may specify $V_{sd}$ and $I_d$ [which fixes $p$ through Eq. (11)] and solve for $s$. As we shall show below, it is often convenient to proceed this way since pertinent small-signal and noise parameters can be conveniently displayed as functions of the normalized drain current $I_d/I_s$. 
It is illuminating to display as functions of the normalized drain current, solution sets for the reduced potentials $s$ and $p$ or equivalently the normalized channel openings at the source and drain ends of the gate, $(1 - s)$ and $(1 - p)$, respectively. Figure 8 is a graph of $(1 - s)$ and $(1 - p)$ as functions of $I_d/I_s$ for various values of the ratio $L/a$ and $\xi$, typical of microwave transistors. In the usual operating range of current, $I_d/I_s$ is of the order of 0.5 or less. Notice that although the channel opening on either end of the gate is a very strong function of the drain current, or equivalently of the gate bias, the percentage variation of the channel width from source to drain is of the order of 10–20%, at most, except at very small currents. In other words, the channel boundary is nearly parallel to the symmetry plane, so that the approximation $s \approx p$ is usually good at high currents, especially for short gate lengths, i.e., $L/a \leq 5$.

The values for $s$ and $p$ are insensitive to the value of the drain potential. On the other hand, the length of the velocity-saturated region $L_2$ is a strong function of $V_{sd}$, though not of the ratio $I_d/I_s$. Figure 9 illustrates the dependence of $L_2$ on $V_{sd}$ for a typical value of $I_d/I_s$ and $\xi$. Note that the length of region II increases with $V_{sd}$. For dimensions typical of microwave devices,
for example $L = 1 \mu m$, $a = 0.3 \mu m$, region II encompasses approximately 96% of the region under the channel for $V_{sd} = W_{oo}$. The strong penetration of the velocity-saturated regime into the gate region, as depicted by Fig. 9 also has been demonstrated numerically by Himsworth (1972) with his two-dimensional computer analysis of the FET. Although we have considered one current ratio, the results depicted in Fig. 9 are typical of other drain current ratios also.

It is interesting to replot the data of Fig. 9 against the ratio $L/a$ for $V_{sd}/W_{oo} = 1$, but with the length of region II normalized to the epitaxial thickness $a$. This is done in Fig. 10. Notice that $L_2/a$ is insensitive to the value of $L/a$ and the saturation index $\xi$. Indeed, one may conclude that the extent of the saturated velocity regime is approximately three times the epitaxial thickness for drain biases of the order of the pinch-off voltage.

C. Small-Signal Parameters

The small-signal equivalent circuit of the FET, valid up to moderately high frequencies, is shown in Fig. 11. In Fig. 11a a perspective sketch indicates the equivalent circuit parameters and the approximate region of the FET responsible for each element. Figure 11b is the corresponding circuit representation. For the present discussion, we shall focus attention on the

![Graph](image-url)

Fig. 9. Relative length of velocity-saturated region as a function of the normalized drain voltage and ratio $L/a$. $I_d/I_s = 0.5$, $\xi = 0.1$. 
intrinsic portion of the FET, the section enclosed by dashed lines, and assume that the parasitic resistances $R_f$, $R_{dr}$, and $R_m$ are absent.

The gain mechanism is embodied in the transconductance $g_m$. The output or drain resistance is represented by the resistor $r_d$. The depletion layer capacitance under the gate electrode is denoted by the source-gate capacitance $C_{sg}$, and its charging resistance in the channel by $R_i$. The parasitic capacitances $C_{ds}$ and $C_{sd}$ represent, respectively, the fringing capacitances between the drain electrode and the gate and source contacts. In the analysis to follow we shall derive expressions for these various circuit elements in terms of the geometric and material parameters and the operating bias conditions.

1. Transconductance $g_m$

The transconductance and drain resistance are evaluated by a perturbation of the dc characteristic resulting from small changes in the applied gate and drain potentials. The transconductance is defined as the ratio of the
small change in drain current produced by a small change in gate voltage when the source-drain voltage $V_{sd}$ is fixed, that is

$$g_m = -\frac{dI_d}{dV_{sg}} \bigg|_{V_{sd}}$$  \hspace{1cm} (19a)

$$= g_0 E_s Z (dp/dV_{sg}) = (g_0 E_s Z/2sW_0)(dp/ds).$$  \hspace{1cm} (19b)

The gate potential, characterized by $s$, causes not only a change in the pinch-off potential $p$ but also of the length $L_1$. Differentiating Eqs. (13) and (18), using the relation $L_1 + L_2 = L$, one may solve for $dp/ds$, and obtain...
the expression

\[ g_m = \left( \frac{I_s}{W_{00}} \right) f_g(s, p, \zeta), \quad (20) \]

where \( f_g \) is the nondimensional function given by

\[
f_g(s, p, \zeta) = \frac{(1 - s) \cosh \left( \frac{\pi L_2}{2a} \right) - (1 - p)}{[2p(1 - p) + \zeta(L_1/L)] \cosh \left( \frac{\pi L_2}{2a} \right) - 2p(1 - p)}.
\]

(21)

In the limit \( L_2 \to 0 \) and \( p = d \), \( g_m = \left( g_0 Z/L \right)(d - s) \), which is van der Ziel and Ero's result (1964).

The normalizing conductance factor

\[ \frac{I_s}{W_{00}} = 4\kappa e_0 v_s(Z/a) \quad (22) \]

is independent of the doping level. To obtain a measure of the magnitude of this factor, let \( Z = 5 \times 10^{-2} \) cm and \( a = 2 \times 10^{-5} \) cm—typical microwave design values. With \( \kappa = 12.5 \) and \( v_s \approx 10^7 \) cm/sec, we obtain \( I_s/W_{00} \approx 100 \) mmho.

The dependence of \( g_m \) on the applied gate and drain potentials is embodied in the function \( f_g \). We have computed \( f_g \) as a function of the normalized drain current for several values of the saturation index \( \zeta \) and geometric ratio \( L/a \) typical of microwave designs. These are shown by the solid lines in Figs. 12a–c for the case \( V_{sd}/W_{00} = 1 \). The transconductance function is insensitive to the ratio \( V_{sd}/W_{00} \) when this ratio is of the order of 0.5 or greater, as would be the case under normal operating conditions.

Observe that although \( g_m \) increases rapidly for large values of drain current, in the practical range corresponding to a reverse-biased gate junction, i.e., \( I_d/I_s \approx 0.5 \) or less, \( f_g \) is only a mild function of current and the ratio \( L/a \), and is of the order of 0.4–0.8. It is also insensitive to the saturation index for the range shown; however, one may show that when velocity saturation becomes unimportant, that is, when \( \zeta \to \infty \), \( g_m \) increases significantly. Thus, for short-gate (microwave) GaAs FETs the most effective way to increase \( g_m \) is to increase the gate width \( Z \), since the conductance factor \( I_s/W_{00} \) varies linearly with this dimension.

The expression for \( g_m \) simplifies considerably for a short-gate device, that is when the approximations \( s \approx p, L_1 \approx 0 \) hold. In this case

\[ g_m \approx \frac{1}{2p} \left[ \frac{I_s}{W_{00}} \right] \quad (23a) \]

\[ = \frac{I_s}{2W_{00}} \left( \frac{1}{1 - I_d/I_s} \right). \quad (23b) \]

The second expression is a remarkably good approximation when \( I_d/I_s > 0.1 \) and is essentially a representation of the confluence of the various graphs of \( f_g \) in Fig. 12 for this current range.
Fig. 12. Transconductance and drain resistance as a function of normalized drain current for several values of the saturation index $\xi$ with the drain voltage fixed. $V_{sd}/W_{oo} = 1$, $g_m = (l_s/W_{oo})f_s$, $r_d = (W_{oo}/l_s)f_r$. (a) $L/a = 3$, (b) $L/a = 5$, (c) $L/a = 10$.

2. Drain Resistance $r_d$

The drain resistance $r_d$ is the ratio of the change in drain voltage to the differential change in drain current producing it when the gate voltage is fixed, that is

$$r_d = -\frac{dV_{sd}}{dI_d} \bigg|_{V_{gs}}.$$  (24)
The negative sign stems from the fact that \( I_d \) is directed outward from the drain contact. By a differential process analogous to that used for \( g_m \), it has been shown by the authors (Statz et al., 1974) that \( r_d \) can be expressed in the form

\[
r_d = (W_{00}/I_s)f_r(s, p, \xi)
\]

where

\[
f_r(s, p, \xi) = \frac{1}{1 - p} \left[ 2p(1 - p) + \xi \frac{L_1}{L} \cosh \frac{\pi L_2}{2a} - 2p(1 - p) \right].
\]

Notice that the quantity in braces is the same as the denominator of \( f_g \). In the limit \( L_2 \to 0, p = d \), the expression (25) reduces to \( r_d = (L/Zg_0) \times (1 - d)^{-1} \) which was obtained by van der Ziel (1962) for the case of no velocity saturation.

Graphs of the resistance function, or rather the product \( \xi(a/L)f_r \), are shown in dotted lines in Figs. 12a–c. Note that at low drain currents \( r_d \) is somewhat more sensitive to \( I_d \) than is \( g_m \). Not only is \( r_d \) sensitive to drain current (gate bias), but it also varies strongly with drain voltage. Curiously enough, the variation with drain voltage at constant drain current is nearly linear over a wide range of drain voltages as Fig. 13 shows. In practical

![Fig. 13. Normalized drain resistance as a function of normalized source-drain bias and the geometric ratio \( L/a \). The curves are drawn for a fixed drain current. \( I_d/I_s = 0.5 \), \( r_d = (W_{00}/I_s)f_r \).](image)
devices, the drain resistance is usually lower than the value computed and is a rather arbitrary function of the operating potentials because of leakage paths on the surface or through the substrate (Reiser, 1970).

For short gate lengths and not too low drain current, the expression for $r_d$ simplifies to

$$r_d \approx \pi \frac{L}{\xi a} \frac{|V_{sd}|}{I_s} p$$

which is independent of the gate length! Note that the linear dependence of $r_d$ on source-drain potential is evident now. Also observe the linear dependence on drain current.

3. Gate-Source Capacitance $C_{sg}$

The gate-source capacitance $C_{sg}$ is the rate of change of the free charge on the gate electrode with respect to the gate bias voltage when the drain potential is held fixed. Actually this ratio represents the sum of the source-gate and drain-gate capacitances, but for practical microwave devices the drain-gate capacitance contribution is relatively small as experimental evidence indicates (Liechti et al., 1972; Baechtold, 1972). Thus we define

$$C_{sg} \approx C_{gg} = dQ_g / dV_{sg} \bigg|_{V_{sd}}.$$  

The gate charge $Q_g$ is the integral over the gate electrode of the field component normal to the electrode. In region I, this field corresponds to the space-charge potential $W(x)$, Eq. (5). However, in region II an additional component of field is introduced by the Laplacian potential $\Phi(x,y)$, Eq. (17). It can be shown (Appendix I) that the resultant charge on both gates is given by the expression

$$Q_g = 2qNaZ \left[ \frac{f_2(s, p)}{f_1(s, p)} L_1 + pl_2 + \frac{\xi a^2}{\pi L} \left( \cosh \frac{\pi L_2}{2a} - 1 \right) \right]$$

where

$$f_2(s, p) = \frac{2}{3}(p^3 - s^3) - \frac{1}{4}(p^4 - s^4).$$
The first term in Eq. (29) represents the contribution of region I. Performing the differentiation indicated by (28), we show in Appendix I that

\[ C_{sg} \approx 2\kappa\varepsilon_0 Z f_c(s, p, \zeta) \]  

(31)

where \( f_c = f_{c1} + f_{c2} + 1.56 \) with

\[ f_{c1}(s, p, \zeta) = \frac{2}{L_1} \left[ f_g \left( \frac{2p^2(1 - p)^2}{1 - p} + f_2 \right) - s(1 - s) \right] \]  

(32a)

\[ f_{c2}(s, p, \zeta) = \frac{2L_2}{a} f_g + (1 - 2pf_g) \times \left[ \frac{2L}{a \zeta \cosh(\pi L_2/2a)} + \tanh(\pi L_2/2a) \right]. \]  

(32b)

In this expression \( f_{c1} \) and \( f_{c2} \) represent the contributions of regions I and II, respectively. The numerical additive term takes into account the fringing capacitance at either edge of the gate electrode as computed by Wasserstrom and McKenna (1970). For short gate lengths of the order of 1 \( \mu \)m, this fringing contribution can account for as much as 25% of the total capacitance. Equation (31) also applies to the asymmetric FET if the factor of 2 is dropped. Typical values of \( C_{sg} \) for a microwave design fall in the range 0.1–1.0 pF.

The capacitance function \( f_c \) or rather \( f_c/(L/a) \) is graphically displayed in Figs. 14a–c as a function of normalized drain current and representative parameter values. Notice that the capacitance function is weakly dependent on the saturation index. For short gate lengths and gate biases not too near the pinch-off value \( W_{00} \), the expression for \( C_{sg} \) becomes particularly simple. For this case, using \( p \approx s, L_1 \approx 0 \), only the first term of \( f_{c2} \) remains and one obtains

\[ C_{sg} \approx 2\kappa\varepsilon_0 Z \left[ \frac{L}{ap} + 1.56 \right] \]  

(33a)

\[ = 2\kappa\varepsilon_0 Z \left[ \frac{L}{a \left( 1 - I_d/I_s \right)} + 1.56 \right] \]  

(33b)

where the first term corresponds to a "parallel-plate" capacitor of thickness \( ap \). Note that \( C_{sg} \) is approximately linearly dependent on gate length, as one might expect. The simplified expression (33b) is an excellent approximation of all three sets of curves displayed in Fig. 14.
4. Drain-Gate and Source-Drain Capacitances $C_{dg}$ and $C_{sd}$

The drain-gate capacitance $C_{dg}$ and source-drain capacitance $C_{sd}$ should be considered parasitic elements of the FET since to first order they are not intrinsic to the gain mechanism of the FET, but rather are fringing capacitances between electrodes. To evaluate them properly, it is necessary to revert to the actual planar geometry, Fig. 5, rather than the idealized symmetric transistor, Fig. 6b, used so far. The proximity of the contacts in the idealized model would yield an overestimate of these capacitances, particularly for the drain-gate capacitance.
A good estimate of these capacitances can be obtained by considering the electrostatic coupling between two parallel conductors on a surface of a semi-infinite dielectric, in this case the GaAs chip, since the interelectrode spacings are small compared to the chip (substrate) thickness. Figures 15a and b are the models to be used in our analysis of $C_{dg}$ and $C_{sd}$.

Smythe (1968) has developed an expression for interelectrode capacitances between parallel strips immersed in an infinite dielectric medium. By properly modifying his expressions to account for the air dielectric above the electrodes, one obtains an approximate expression for the capacitance applicable to both $C_{dg}$ and $C_{sd}$ of the form

$$C_{dg}, C_{sd} = (k + 1)\varepsilon_0 Z K(1 - k^2)^{1/2}$$

where $K(k)$ is the complete elliptic integral of the first kind. Equation (34), of course, applies only to the asymmetric FET. The argument $k$ for each capacitance is given below

$$k_{dg} = \left(\frac{L_{dg}}{L_{dg} + L_d}\right)^{1/2}$$

$$k_{sd} = \left[\frac{(2L_s + L_{sd})L_{sd}}{(L_s + L_{sd})^2}\right]^{1/2}$$

where $L_{dg}$ and $L_{sd}$ are, respectively, the interelectrode spacings between the drain contact and the gate and source electrodes. In these expressions, it has been assumed that the length of the drain electrode $L_d$ is large compared to the length of the gate electrode $L_d \gg L$, a good approximation, and that the length of the drain and source electrodes (assumed equal, $L_s = L_d$) are large compared to their spacing, $L_d \gg L_{sd}$, which is also true for practical devices.

Since expression (34) does not involve the FET mechanism, obviously $C_{dg}$ and $C_{sd}$ are independent of operating potentials. For $C_{sd}$, generally speaking, this is consistent with experiment; however, a weak dependence on
bias conditions is observed for $C_{dg}$. Experimentally, good agreement is obtained with the theoretical value of $C_{sd}$, even though the shielding action of the gate electrode has been ignored. Calculated values of $C_{dg}$ appear to be somewhat higher than the experimental values; therefore, the analytic value for $C_{dg}$ should be considered an upper bound. Typical values of $C_{dg}$ and $C_{sd}$ for a 500 $\mu$m wide gate are 0.03 pF and 0.06 pF, respectively.

Figures 16a and b illustrate the dependence of $C_{dg}$ and $C_{sd}$ on electrode dimensions and spacings. Note that $C_{dg}$ does not depend strongly on gate length and is a rather mild function of interelectrode spacing. The source-drain capacitance is nearly independent of interelectrode spacing for the practical range plotted, and is a weak function of electrode size.

### III. The FET with Parasitic Resistances

One may modify the preceding dc and small-signal analyses to include the ever-present parasitic contact and bulk resistances between the edges of the gate electrode and the source and drain contacts. These are denoted, respectively, as $R_f$ and $R_{dr}$, and are indicated in the schematic of the planar FET, Fig. 11. It is assumed that these resistances are the same for both the signal and the dc response.

Let us consider first the effect on the dc characteristics. Since the drain current passes through both resistances, it will have the effect of dropping part of the externally applied drain-source bias, here denoted by the symbol $V_{dd}$, to the internal level $V_{sd}$ by an amount $I_d(R_f + R_{dr})$. Thus we have the relation

$$V_{sd} = V_{dd} - I_d(R_f + R_{dr}).$$

In addition the potential drop across $R_f$ serves to "back-bias" the gate electrode so that we have the relationship

$$V_{sg} = V_{ss} + I_d R_f$$

where $V_{ss}$ is the externally applied gate-source bias. If one inserts these two expressions into Eqs. (18) and (2a), respectively, then it is possible to derive the terminal $I$–$V$ dc characteristics of the FET once the values of $R_f$ and $R_{dr}$ are known.

It is not easy to model these resistances analytically, and even if this were possible, the variability of interfacial contact resistances due to process variations would negate the usefulness of the model. Rather, it is more fruitful to obtain these resistances experimentally, by measuring the slope of the $I_d$–$V_{dd}$ characteristic near the origin as a function of gate bias and correct for the channel resistance contribution. A method for doing this has been described recently by Hower and Bechtel (1973). Typically, values of $R_f$ and $R_{dr}$ fall in the range from 5–20 $\Omega$, depending on the gate width. Usually $R_{dr}$ is greater...
FIG. 16. Theoretical dependence of parasitic capacitances on electrode dimensions and spacings. (a) Drain-gate capacitance $C_{dg}$, (b) Source-drain capacitance $C_{sd}$. 
FIG. 17. Comparison between the calculated and measured drain current-voltage characteristic for an X-band GaAs FET. The dashed line represents the locus of operating bias voltages at the onset of velocity saturation. To the right of the line, velocity saturation becomes important. $N_d = 6.5 \times 10^{16} \text{ cm}^{-3}$; $\alpha = 0.34 \mu\text{m}$; $Z = 500 \mu\text{m}$; $L = 1.0 \mu\text{m}$; $R_f = 6.5 \Omega$; $R_{dr} = 11.3 + f(V_{ds}) \Omega$ (---) Theory, (○) experiment.

than $R_f$ because of the wider interelectrode spacing between the gate and drain electrodes.

Figure 17 demonstrates the excellent agreement obtained between calculated and measured dc characteristics for an X-band device having a 1.0 $\mu\text{m}$ gate length. The parasitic resistances were determined by Hower's method, but an heuristically determined voltage dependence of $R_{dr}$ was necessary as indicated in the legend of Fig. 17. The locus $L_2 = 0$ represents the operating bias values corresponding to the onset of velocity saturation at the drain end of the channel. It is evident that in the current saturation regime, $V_{dd} > 2 \text{ V}$, velocity saturation occurs for all values of the applied gate and drain biases. One usually operates an FET in this region. Note the nonzero slope (finite drain resistance) predicted for the region above the knee of the characteristics.

The small-signal performance is affected by $R_f$ as a negative feedback, analogous to the degeneration produced by an unbypassed cathode resistance of a vacuum tube. This feedback reduces the internal $g_m$ to a terminal value $g_m^\ast$ given by

$$g_m^\ast = g_m/(1 + g_m R_f).$$

(38)
This feedback is most pronounced at low gate bias voltages, that is, when $g_m$ is high. For a well-designed microwave device, $g_m^*$ is within 20–30% of the internal value.

The parasitic drain contact resistance can be neglected, insofar as small-signal performance is concerned, since it is always small compared with the drain output resistance. An additional parasitic resistance, which though unimportant for dc considerations, must be included in the small-signal equivalent circuit, is the resistance of the thin gate-metallization, represented by $R_m$ in Fig. 11. This resistance, which may exhibit the skin effect, taken together with $R_f$ has a pronounced effect not only on the input resistance at high frequencies but perhaps more importantly, on the noise figure, since it is a source of thermal noise. Indeed $R_f$ and $R_m$ are the major sources of external noise in a GaAs microwave transistor, as we shall show later.

Figure 18 is a comparison of the calculated and measured source-gate capacitance and transconductance for the device whose dc characteristics are displayed in Fig. 17. As can be seen, the theoretical model agrees very well with the data points.

![Graph showing the comparison between theoretical and experimental values of the source-gate capacitance $C_{gs}$ and terminal transconductance $g_m^*$](image)

**Fig. 18.** Comparison between the theoretical and experimental values of the source-gate capacitance $C_{gs}$ and terminal transconductance $g_m^*$. The applied drain bias $V_{dd}$ is held fixed ($V_{dd} = 3.0$ V) and the gate bias $V_{gs}$ is varied. $N_a = 6.5 \times 10^{16}$ cm$^{-3}$; $a = 0.34 \mu$m; $Z = 500 \mu$m; $L = 1.0 \mu$m; $R_f = 6.5 \Omega$ (—) Theory, (○) experiment.
IV. Noise

A. Introduction

1. The Intrinsic Noise Sources

Noise in a microwave GaAs FET is produced both by sources intrinsic to the device and by thermal sources associated with the parasitic resistances. The intrinsic noise arises from two mechanisms. The first of these is the thermal or Johnson noise produced in the "ohmic" section of the channel, that is, region I. This source has been analyzed for the JFET by van der Ziel (1962, 1963a) and for the MOSFET by Shoji (1966). The second mechanism is the diffusion noise in the velocity-saturated section of the channel, region II. This noise mechanism, which has not been included in FET analyses before, can be the dominant one for short-gate devices as we shall show.

Before we proceed with our noise analysis, it may be appropriate at this point to digress briefly to consider, in somewhat general terms, the distinction between the noise generated in an ohmic conductor and the noise produced in a conductor supporting velocity limited carrier flow. This will serve to establish the physical basis for the noise analysis.

The constitutive law of conduction relating the one-dimensional current density \( j \) to the electric field \( E \) and the density gradient \( \partial n / \partial x \) is given by

\[
  j = \sigma E + qD(\partial n / \partial x) + j_n
\]

(39)

where \( j_n \) represents the noise generating mechanisms. The noise generating mechanisms at different spatial positions are uncorrelated. As shown by Shockley et al. (1966) and by van der Ziel and van Vliet (1968), the spectrum of \( j_n \) is given by

\[
  j_n(x)j_n^*(x') = 4q^2(Dn/A)\Delta f \delta(x - x')
\]

(40)

where \( A \) is the cross-sectional area of the conductor, in our case the channel. This is a general result and applies even if the diffusion coefficient is a function of the electric field.

The delta function appearing in this expression must be interpreted to be zero, for \( x \neq x' \), and equal to \( 1/\Delta x \) when \( x = x' \), where \( \Delta x \) is the length of the incremental sections into which the conduction region has been partitioned for the purpose of analysis. (In the limit \( \Delta x \) will be made to approach the differential length \( dx \).) The source becomes very large as \( \Delta x \) is made small. This is a natural consequence of the fact that statistical fluctuations in a system increase with the decrease of system size. In order to be consistent with the assumptions made in deriving Eq. (40), one must choose \( \Delta x \) to be
nonzero but small compared with the macroscopic dimensions of the system.

Instead of re-deriving (40) here, we shall show that it is physically plausible in that it leads to the familiar Nyquist or Johnson noise formula for a conductor obeying Ohm's law. We will then show how it can be used to explain the noise generating mechanism in the strongly non-ohmic case of carrier velocity saturation.

For an ohmic conductor, the diffusion coefficient is independent of the applied field and is related to the low-field mobility \( \mu_0 \) by the Einstein relationship \( D = D_0 = (kT/q)\mu_0 \), hence the identity

\[
q^2 D n/kT = \sigma
\]  

(41)

holds. This relation transforms the general law (40) into the more familiar special case

\[
\frac{\partial}{\partial t} j_n(x) j_n^*(x') = 4(\sigma/A)kT \delta(x - x').
\]  

(42)

We shall show now that this expression is consistent with the well-known Nyquist formula for a conductor of resistance \( R \) at thermal equilibrium. For this purpose one must restrict the analysis to processes of sufficiently high conductivity and low concentration gradient so that the diffusion term in Eq. (39) can be neglected. If the conductor is open-circuited, that is if \( j = 0 \), then at low frequencies \( E = -j_n/\sigma \), where \( j_n \) constitutes a set of mutually uncorrelated, randomly activated spatial impulse functions extending from \( x \) to \( x + \Delta x \), of "content"

\[
j_n \Delta x = (4\sigma kT \Delta f / A)^{1/2} (\Delta x)^{1/2}
\]  

(43)

assigned to the frequency increment \( \Delta f \). The open-circuit mean square voltage is obtained as the mean square superposition of the voltages \( E \Delta x \) produced by each of these sources. Thus

\[
|v^2| = \sum |E \Delta x|^2 = \frac{4kT \Delta f}{\sigma A} \sum \Delta x = 4RkT \Delta f
\]  

(44)

where \( R = L/\sigma A \) is the resistance and \( L = \sum \Delta x \) is the length of the conductor. This is the well-known Nyquist formula.

In his theory of FET noise, van der Ziel used the Nyquist law with \( T \) assumed independent of position. When the carriers are driven by an \( E \)-field, their random velocities may increase above the values corresponding to the lattice temperature and hence their temperature \( T \) is greater than the lattice temperature. To the extent that the carriers have an (electric-field produced) average velocity small compared with their random velocities, their statistical properties may still be assumed to be those of thermal equilibrium but at the elevated carrier temperature. For this reason one may introduce into the
constitutive law a Gaussian noise source whose spectrum is derived on the basis of equilibrium considerations, the rise in carrier temperature being taken into account by treating $T$ as a function of the local $E$-field. The implications of a field-dependent carrier temperature were considered briefly by Klaassen (1971) and by van der Ziel (1971a,b) for FETs in which velocity saturation was assumed absent. The first detailed quantitative treatment incorporating hot electron temperatures in a noise analysis was made by Baechtold (1971, 1972) for Si and GaAs devices. However, Baechtold did not include a second velocity-saturated region in his model.

The treatment of the noise in region $I_1$ is completely different from the above. Here the carriers drift at their saturated velocity $v_s$, and Ohm’s law no longer holds. Yet, interestingly enough, the noise sources may still be obtained from quasi-equilibrium considerations as we shall argue below. The basis for our discussion, however, is no longer the specialized form, Eq. (42), but the general equation (40).

When the electric field has increased the carrier energy so that an appreciable number of carriers have energies comparable to the optical phonon energy, an increase in the electric field will cause energy transfer from the carriers to the lattice without a change in the carrier drift velocity. This, of course, is the phenomenon of velocity saturation. Even under this condition the rapid randomization of the direction of carrier velocity is sufficient to maintain a roughly spherical velocity distribution in velocity space. To the extent that a roughly spherically symmetric velocity distribution (in a frame of reference moving at the carrier drift velocity) implies a random walk process, the noise source $j_n$, described by Eq. (40), associated with the velocity-saturated carrier flow, can be attributed to charge displacements produced by the random motion of the carriers. This, of course, is the process responsible for diffusion. Hence, the carriers still experience diffusion, even though their response to a change in the electric field has been eliminated for the most part. According to Eq. (40) the current spectrum is white. Hence, at any position $x$ within the spatial increment $\Delta x$, the microscopic currents $i_n(x) = j_n(x)\Delta$ occur in short bursts, uncorrelated from one instant of time to the next. A current burst within the spatial interval $x$, $x + \Delta x$, leads to a charge displacement from $x$ to $x + \Delta x$, resulting in an electric dipole layer with one charge sheet at $x$, and equal and opposite charge sheet at $x + \Delta x$.

When diffusion is dominant and ohmic conduction absent in a reference frame moving with the average velocity $v_s$, the constitutive law can be used but with $\sigma = 0$. This indicates that a displacement of charge, with an attendant gradient of carrier density, produces a diffusion current component. Since a dipole layer is highly singular, one might expect that the associated diffusion current $qD(\partial n/\partial x)$ would in time greatly alter the carrier distribu-
tion in the dipole layer. This is indeed the case; however, in a low frequency noise analysis only the lowest spatial Fourier components of the drifting dipole layer density contribute to the noise. These Fourier components may be shown to experience negligible diffusion during the transit time within the drift region. For this reason one may compute the induced gate noise on the basis of dipole layers drifting undisturbed at the saturated velocity $v_s$ provided one restricts the analysis to "low frequency" noise. This is the foundation for the authors' treatment of the noise originating in region II. The interpretation of high field noise in FETs as diffusion noise has been suggested by van der Ziel (1971b) also, but he did not consider the case of velocity saturation.

It is convenient for noise figure calculations to represent the internal noise sources of the intrinsic FET by noise generators suitably connected to the external terminals of the intrinsic FET (now considered noiseless). One may do this for any linear two-port (Rothe and Dahlke, 1956). A particularly convenient representation which relates closely to the physical noise generating process in the FET is a pair of noise current generators, one connected across the input port (gate-source) and one connected across the output port (drain-source). These are labeled as $i_g$ and $i_d$, respectively, in Fig. 19a. The

![Diagram](image)

**FIG. 19.** Representation of a noisy FET by terminal noise sources. (a) Intrinsic FET with two noise sources. The current source $i_g$ represents the induced gate noise, the output current source $i_d$, the drain circuit noise. (b) The intrinsic FET with parasitic resistances. The voltage generator $e_m$, represents the thermal noise of the gate contact resistance $R_m$, the voltage generator $e_r$, the thermal noise of the source contact resistance $R_r$. 
direction of the current generators follows the convention adopted by van
der Ziel. The representation in terms of external current generators is useful
because the output generator can be identified with the short-circuit channel
noise generated in the source-drain path, while the input generator can be
related to the noise current induced in the gate circuit by the charge fluctua-
tions in the drain current. Because of the coupling between the drain noise
and the gate noise, the current generators are partially correlated.

2. The Extrinsic Noise Sources

A practical FET always contains additional noise sources external to the
intrinsic FET which are associated with the parasitic resistive paths in series
with the terminals. These sources generate Johnson noise and can be ex-
pressed in terms of the resistance values. For a microwave FET there are two
principal sources of parasitic noise. These are illustrated in Fig. 19b. The
first, represented by the voltage generator $e_m$ arises from the thermal noise
produced in the gate metallization resistance $R_m$. Usually this contribution
is not negligible for microwave FETs because the resistance of the thin films
used for the gate fingers cannot be neglected. The second source, labeled $e_r$
is associated with the gate-source path resistance $R_r$ external to the channel.
(See Fig. 11.) The drain contact resistance $R_{dr}$ (Fig. 11) also generates ther-
mal noise, but this source can be neglected in comparison with the other
sources after amplification. When the FET is connected into a circuit, addi-
tional thermal noise is generated by the lossy circuit elements. These must be
taken into account when one computes the noise figure of an FET amplifier;
however, we do not associate these noise sources with the FET.

3. A Synopsis of the Noise Analysis

It will be our principal objective in the present section to analyze the
various internal noise mechanisms contributing to the current generators
and to obtain analytic expressions for this noise. Specifically, we shall obtain
analytic representations for the mean square values $\langle i_g^2 \rangle$, $\langle i_d^2 \rangle$ where the
overbar indicates a statistical average, and for the correlation coefficient $JC$
defined by the relation

$$JC = \frac{i_g^* i_d}{(\langle i_g^2 \rangle \langle i_d^2 \rangle)^{1/2}}$$

where the asterisk denotes the complex conjugate and $j = (-1)^{1/2}$.

Our analysis is restricted to frequencies below which transit-time effects
in the channel play a major role (a reasonable assumption for present
microwave FETs); therefore, the transconductance $g_m$ and the spectrum of
The signal and noise properties of GaAs FETs are independent of frequency. Since $i_g$ is produced by capacitive coupling of the gate circuit to the noise sources in the drain circuit, $|i_g^2|$ will vary as frequency squared, i.e. as $\omega^2$, and $i_g^*i_d$ as $\omega$, where $\omega = 2\pi f$ denotes the radian frequency. Therefore, the correlation coefficient is imaginary and independent of frequency.

The analysis of the internal noise will be somewhat complex, and to make it easier to understand, it will be useful to outline briefly the method of presentation. In the first part, Section IV,B, we will derive an expression for the open-circuit noise voltage $|v_d^2|$ developed across the source-drain path, and by the simple circuit transformation $i_d^2r_d^2 = |v_d^2|$, we shall convert this voltage to the equivalent noise current generator. (It is convenient to proceed from the open-circuit voltage, because all incremental noise voltage fluctuations distributed along the channel are in series and can be added.)

The determination of $|v_d^2|$ will begin with a calculation of the thermal noise generated in region I. In this analysis we shall draw heavily on the earlier work of van der Ziel (1962, 1963a). However, we will add two new features to van der Ziel's treatment to apply it to the GaAs FET. First, we include the field dependence of the noise temperature of the (hot) electrons, as suggested by Baechtold (1972). Second, we take into account the enhancement of this thermal noise as it propagates through region II. Let the voltage fluctuation developed across region I be called $v_1$. Then by its modulation of the position of the joining plane $x = L_1$, $v_1$ is amplified as it appears at the far end of the velocity-saturated region. Let the resultant open-circuit noise voltage be denoted by $v_{d1}$.

Proceeding to region II, we investigate the noise mechanism under velocity-saturated conditions. Unlike region I, the noise here is attributed to spontaneous generation of dipole layers, rather than Johnson noise. We integrate this distributed noise over region II and obtain a mean square voltage contribution, $|v_{d2}^2|$. Since this noise source is not correlated with the Johnson noise produced by region I, the total mean square drain voltage is the sum of $|v_{d1}^2|$ and $|v_{d2}^2|$. Thus the short-circuit drain current noise is

$$|i_d^2| = (|v_{d1}^2| + |v_{d2}^2|)/r_d^2. \quad (46)$$

In the next step in our analysis, Section IV,C, we derive expressions for the induced gate noise produced by the elementary noise voltage fluctuations in the channel. The approach used here is to assume short-circuited drain conditions, as van der Ziel does, and to interpret the resulting fluctuations of the drain current $i_d$ as charge fluctuations in the channel. These charge fluctuations produce opposite charge fluctuations on the gate electrode which can be expressed in terms of the short-circuited gate current $i_g$. We begin by calculating the induced gate charge produced by Johnson noise generated in region I. The elementary noise voltage fluctuations in this
region induce charge fluctuations on the gate electrode via two coupling mechanisms, one local, involving region I only, the other remote, involving region II. In the first coupling the noise fluctuations cause, locally, a channel width fluctuation, or equivalently a depletion layer charge fluctuation. The latter induces an equal but opposite charge fluctuation on the segment of the gate electrode in region I adjacent to the channel height fluctuation. This is the mechanism invoked by van der Ziel (1963a) in his treatment of gate noise in FETs with no velocity saturation. The indirect coupling to region II occurs somewhat differently, although channel height modulation is also involved. The component of the short-circuit drain current fluctuation produced by the noise sources in region I, namely \( i_{d1} = v_{d1}/r_d \), requires that the entire (uniform) channel height in region II fluctuate or "breathe" in synchronism with this current fluctuation because of the saturation of the carrier velocity. This channel height modulation, like that in region I, also requires a compensating fluctuating charge on the gate electrode segment in region II.

The two charge fluctuation components are fully correlated. If we define the direct component of induced gate charge, \( q_{11} \) and the indirect component \( q_{12} \), then the total charge \( q_{g1} \) induced on the gate by fluctuations in region I is

\[
q_{g1} = q_{11} + q_{12}.
\]  

We next determine the induced charge fluctuations produced by the diffusion noise of region II. Since a dipole layer carries no net charge, it cannot couple a charge directly onto the elementary gate segment in region II adjacent to the dipole, unlike the direct charge induction that takes place in region I. However, indirectly the dipole can couple a charge over the entire gate length, via the short-circuit drain current fluctuations \( i_{d2} = v_{d2}/r_d \) produced by the dipole induced voltage drop \( v_{d2} \) generated in region II. The indirect coupling is by the same channel height "breathing" mechanism discussed earlier for \( q_{12} \). Let \( q_{g2} \) denote the total induced gate charge produced by the dipoles. Since this charge fluctuation is uncorrelated with \( q_{g1} \), the mean square gate charge fluctuation \( |q_g^2| \) is given by

\[
|q_g^2| = |q_{g1}^2| + |q_{g2}^2|.
\]  

The short-circuit mean square gate noise \( |i_g^2| \) can be obtained from the above by the relation

\[
|i_g^2| = |i_{g1}^2| + |i_{g2}^2|.
\]  

where \( |i_{g1}^2| = \omega^2 |q_{g1}^2| \) and \( |i_{g2}^2| = \omega^2 |q_{g2}^2| \).

Finally, in Section IV,D, using the results outlined above, we calculate the correlation coefficient \( jC \), Eq. (45). We now proceed to the calculation of the various noise components.
B. Drain Circuit Noise

1. Open-Circuit Drain Voltage Fluctuation Produced by Sources in Region I

The mean square noise voltage developed across region I by thermal fluctuations can be taken from the treatment of van der Ziel (1962). The rms voltage fluctuation at the end of region I produced by an infinitesimal section of channel of length $\Delta x$ at position $x$ is proportional to the incremental channel resistance at that point, corrected for the field-dependent electron temperature $T_e(x)$. The result expressed in terms of the reduced channel potential $w(x)$ is shown in Appendix II to be

$$\left| \Delta v_1^2 \right| = \frac{8kT_e(x)\Delta f W_{00}}{I_d(1 - p)^2} (1 - w)^2 w \, dw$$

(50)

where we have taken the limit $\Delta x \rightarrow dx$. For $T_e$ we employ the expression proposed by Baechtold (1972) based on his experimental results,

$$T_e/T_0 = 1 + \delta(E/E_s)^3$$

(51a)

where $T_e$ is the effective noise temperature, $T_0$ is the zero-field temperature, assumed to be 300°K, $\delta$ is an empirical constant, $E$ is the electric field, and $E_s$ is the saturation field. In terms of the reduced potentials,

$$T_e(x) = T_0 \left[ 1 + \delta \left( \frac{1 - p}{1 - w} \right)^3 \right]$$

(51b)

where for $E(x)$ we have used the relation

$$E(x) = E_s \left( \frac{1 - p}{1 - w} \right)$$

(52)

obtained from Eqs. (5), (6), and (11).

Next we evaluate the open-circuit voltage fluctuation at the end of region II attributable to $\Delta v_1$. Because the drain fluctuation current is zero under the assumed open-circuit drain conditions, the width of the channel in region II is fixed, as determined by the direct current $I_d$ and so is the channel voltage $W_p$ at the pinch-off point. It follows that the only parameter that can vary is the position of the pinch-off point $L_1$, that is, the length of region I. The field at $x = L_1$ by definition is equal to the saturation value $E_s$; therefore, the change in length $\Delta L_1$, required to absorb the noise voltage fluctuation $\Delta v_1$ is given by

$$\Delta L_1 = \Delta v_1 / E_s.$$
The source-to-drain fluctuation $\Delta v_{d1}$ resulting from this position modulation can be obtained from Eq. (18) as

$$\Delta v_{d1} = dV_{sd}/dL_1 \left|_{s, p} \right. \quad \Delta L_1 = \Delta v_1 \cosh \left( \frac{\pi L_2}{2a} \right)$$

(54)

where we have used the relation $L_1 + L_2 = L$. The hyperbolic factor represents the "enhancement" of the Johnson noise by region II.

The mean square noise voltage $\langle v_{d1}^2 \rangle$ is obtained by integration of $|\Delta v_{d1}^2|$ over region I, $0 \leq x \leq L_1$ or, equivalently, $s \leq w(x) \leq p$. One obtains (Statz et al., 1974)

$$\langle v_{d1}^2 \rangle = \frac{4kT_0 A_f}{(g_0 Z/L_1)(1 - p)^2} \cosh^2 \frac{\pi L_2}{2a}. \quad (55)$$

The quantities $P_0$ and $P_\delta$ are defined as

$$P_0 = (f_i)^{-1} \left[ (p^2 - s^2) - \frac43 (p^3 - s^3) + \frac12 (p^4 - s^4) \right] \quad (56)$$

and

$$P_\delta = 2\delta (f_i)^{-1} (1 - p)^3 \left[ (s - p) + \ln \frac{1 - s}{1 - p} \right]. \quad (57)$$

Equation (55) also holds for the asymmetric transistor provided the value of $g_0$ appropriate for the one-sided device is used.

The portion of $\langle v_{d1}^2 \rangle$ containing $P_0$ is identical to Eq. (13) of van der Ziel's paper (1962). The new term proportional to $P_\delta$ represents the hot electron contribution.

2. Open-Circuit Drain Voltage Fluctuation Produced by Sources in Region II

We are dealing here with a region in which carriers are drifting at their saturated velocity. As stated earlier, the noise for this condition should properly be interpreted as diffusion noise. The authors have shown elsewhere (Statz et al., 1974) that this diffusion noise may be represented as a uniform distribution of spontaneously generated dipole layers of strength $qAx_0/A$ created at the rate $r = (2DnA)/Ax_0$, where $A = 2(1 - p)aZ$ represents the cross-sectional area of the channel and $n = N$ the density of carriers. As explained earlier, we may assume that these dipoles drift unchanged from their point of generation at $x = x_0$, where $L_1 < x_0 < L$, to the drain electrode $x = L$. Since to the authors' knowledge the analytic treatment of diffusion noise in the velocity-saturated drift region of an FET is new, a somewhat detailed analysis will be presented here.
The potential field associated with a dipole layer of strength \( q \Delta x_0 / A \) situated at the plane \( x = x_0 \) in region II can be expanded in a two-dimensional space harmonic series, each term of which decays exponentially in magnitude in the \( x \)-direction on either side of the plane of the dipole layer. Because of the rapid rate of decay of the higher order terms, the dipole layer potential \( \Psi(x, y) \) can be approximated very well by the first term of this series, namely

\[
\Psi(x, y) \approx \pm \frac{2}{\pi \kappa \varepsilon_0} \left( \frac{q \Delta x_0}{A} \right) \sin \frac{\pi b_p}{2a} \cos \frac{\pi y}{2a} \exp \left( -\frac{\pi}{2a} |x - x_0| \right)
\]  

(58)

where the \((+\)) sign applies for \( x < x_0 \), and the \((-\)) sign for \( x > 0 \).

This dipole potential, by itself, will upset the potential and field at the joining plane of regions I and II which were established by the Laplacian field \( \Phi(x, y) \) to satisfy the boundary conditions there. Therefore a compensating potential will be induced on the open-circuited drain electrode to restore the boundary conditions. Taking into account the drifting of the dipole layer toward the drain, one may show that the compensating (time-dependent) potential disturbance induced on the drain electrode by the dipole has the form

\[
\Delta v_{d2} = -\frac{2}{\pi \kappa \varepsilon_0} \left( \frac{q \Delta x_0}{A} \right) \sin \frac{\pi b_p}{2a} \exp \frac{\pi}{2a} \left[ L - x_0 - v_d(t - t_0) \right]
\]  

(59)

which is valid for \( 0 \leq t - t_0 \leq (L - x_0)/v_s \).

The spectral density of this pulse has frequency components extending up to and beyond the range corresponding to the inverse transit time of region II, namely \( L_2/v_s \). Since we are not interested in frequencies this high, we need concern ourselves only with the spectral density at low frequencies, where the density is flat and corresponds to "white" noise.

Equation (59) represents the induced voltage of one of the many dipoles generated at the plane \( x = x_0 \). Since the dipoles are generated at random times at this plane, they are completely uncorrelated. To obtain the mean square value of \( \Delta v_{d2} \), we must first evaluate the spectral density of one pulse (at low frequencies, \( \omega \to 0 \)) and multiply this by the rate of dipole generation \( r \). Doing so one may show (Statz et al., 1974) that

\[
\left| \Delta v_{d2}^2 \right| = \frac{32 a^2}{\pi^4 v_s^2 (k \varepsilon_0)^2 b_p Z} \sin^2 \left( \frac{\pi b_p}{2a} \right) \left[ \exp \left( \frac{\pi}{2a} (L - x_0) \right) - 1 \right]^2 \, dx_0
\]  

(60)

in the differential limit. We obtain the total mean square voltage produced
by dipoles throughout region II by integrating (60) over the range $L_1 \leq x_0 \leq L$. There results

$$|v_{d2}^2| = I_d \frac{16a^3}{\pi^5 v_s^3 (\kappa e_0)^2 b_p^2 Z^2} \sin^2 \left(\frac{\pi b_p}{2a}\right)$$

$$\times \left[ \exp \frac{\pi L_2}{a} - 4 \exp \frac{\pi L_2}{2a} + 3 + \frac{\pi L_2}{a} \right]. \quad (61)$$

For the asymmetric transistor, the numerical factor of 16 must be replaced by 64, provided $I_d$ is then interpreted as the channel current for the one-sided transistor.

Notice that $|v_{d2}^2|$, unlike $|v_{d1}^2|$, depends explicitly on the drain current, increasing with it and is proportional to the high field diffusion coefficient. We shall see the implications of this later.

Since the noise voltage contributions of the two regions are uncorrelated, their mean square values add. Thus the equivalent short-circuit current generator $i_d$ across the drain-source terminals Fig. 19a consists of the components

$$i_{d1} = \frac{v_{d1}}{r_d}$$

$$i_{d2} = \frac{v_{d2}}{r_d} \quad (62a)$$

$$\text{where } |i_{d1}^2| + |i_{d2}^2| = |i_d^2|.$$  

C. Gate Circuit Noise

1. Short-Circuit Gate Current Fluctuations Produced by Sources in Region I

We have shown in Section IV,B that there are noise voltage fluctuations along the channel. Since the gate is capacitively coupled to the channel, there will be noise charges induced on the gate. These charges are time dependent; therefore there will be noise currents in the gate circuit.

Van der Ziel has evaluated these noise currents for the nonsaturated transistor by setting the noise voltage equal to zero at the end of the ohmic region. Because of the additional velocity-saturated region the boundary conditions at the end of region I are different in the present case.

When we evaluate the induced gate current, we have to add effects due to the "breathing" of the channel in region II. Finally we have to allow for a field-dependent noise temperature.

When proper account is taken of the modified boundary conditions at the end of region I, van der Ziel's expression for the induced gate charge
\[ \Delta q_{11} = (2aqNZL_1/r_d I_d)[ -k + \gamma w(x_0)] \Delta v_{d1} \] 

where \( \Delta v_{d1} \) is the open circuit drain voltage fluctuation corresponding to the elementary voltage fluctuation at \( x_0 \). (Observe that the factor \( \Delta v_{d1}/r_d \) is simply the short-circuit drain current \( I_{d1} \) resulting from the elementary fluctuation.) The parameters \( k \) and \( \gamma \) are given by

\[ k = \left( f_1 \right)^{-1} \left[ -\frac{1}{3}(p^3 - s^3) + \frac{1}{6}(p^4 - s^4) + (s^2 - \frac{2}{3}s^3)(p - s) \right] + \gamma p \] 

(64)

\[ \gamma = 1 + 2p(1 - p) \frac{W_{00}}{E_s L_1} \left[ 1 - \frac{1}{\cosh (\pi/2a)L_2} \right] \] 

(65a)

\[ \gamma = \frac{(1 - p)^2 f_1}{f_1 \cosh (\pi/2a)L_2} \] 

(65b)

The parameter \( \gamma \) represents the modification of van der Ziel's boundary condition at the end of region I. When velocity saturation is absent, i.e., when \( L_2 = 0 \) and \( p = d \), \( \gamma \) becomes unity and the expression for \( \Delta q_{11} \) reverts to van der Ziel's result (1963a).

We remind the reader that in our case \( \Delta q_{11} \) represents the induced charge appearing on that portion of the gate electrode adjacent to region I. To this we must add an additional component \( \Delta q_{12} \) induced on the remaining segment of the gate electrode. As we mentioned earlier, this contribution originates from the "breathing" of the channel height in region II in response to the current fluctuation \( \Delta i_{d1} \). Since the velocity of the carriers is saturated, this current fluctuation demands that the depletion layer give up (or retrieve) additional carriers with a charge per unit length of \( \Delta i_{d1}/v_s \). The induced charge on the gate, therefore, is of opposite sign, thus

\[ \Delta q_{12} = - (\Delta i_{d1}/v_s) L_2 = -(\Delta v_{d1}/r_d v_s) L_2 \] 

(66a)

\[ = -\left[ 2aqNZ(1 - p)L_2/r_d I_d \right] \Delta v_{d1} \] 

(66b)

where we have used the relation \( I_d = 2aqNZv_s(1 - p) \).

This charge is fully correlated with \( \Delta q_{11} \) since it arises from the same elementary disturbance. Adding the two induced charges, we obtain

\[ \Delta q_1 = \Delta q_{11} + \Delta q_{12} \]

\[ = (2aqNZL_1/r_d I_d)[ -k + \gamma w(x_0)] \Delta v_{d1} \] 

(67)
where $\Delta q_1$ is the total induced gate charge caused by an elementary noise voltage fluctuation in region I. The modified parameter $k'$ is given by

$$k' = k + \frac{L_2}{L_1}(1 - p).$$

(68)

The mean square value of this charge can be evaluated after we express $\Delta v_{d1}$ as a function of position. This voltage is proportional to the thermal voltage fluctuation $\Delta W_{x_0}$ at $x_0$, as shown by van der Ziel (1962) and also in Appendix II, modified by the enhancement factor $\cosh \left( \frac{\pi L_2}{2a} \right)$. We find

$$\Delta v_{d1} = -\Delta W_{x_0} \frac{1 - w}{1 - p} \cosh \frac{\pi L_2}{2a}. \quad (69)$$

The elementary voltage fluctuation has a mean square value expressible in terms of the channel resistance of an incremental section $\Delta x_0$ as

$$\frac{\Delta W_{x_0}^2}{\Delta x_0} = \frac{4kT_e(x_0)\Delta f}{2\sigma b(x_0)\bar{Z}} \Delta x_0. \quad (70a)$$

where $T_e$ is the elevated carrier temperature at $x_0$. Proceeding to the differential limit and using the identities $E(x_0) \, dx_0 = dW = 2W_0 w \, dw$ and $I_d = 2\sigma b(x_0)\bar{Z}E(x_0)$, this becomes

$$\frac{\Delta W_{x_0}^2}{\Delta x_0} = \frac{8kT_e(x_0)W_0 \Delta f}{I_d} \frac{\Delta x_0}{dW} \, dw. \quad (70b)$$

Taking the mean square value of (67), using (69) and (70b), and integrating over the range $s \leq w \leq p$, one obtains $|q_{g1}^2|$. The mean square value of the corresponding induced short-circuit gate current $|i_{g1}^2|$ is obtained by multiplication by $\omega^2$; thus

$$|i_{g1}^2| = \omega^2 \frac{64kT_0 \Delta f}{g_0/(L_1 Z)} \left( \frac{\kappa e_0 L_1}{\gamma a} \right)^2 (R_0 + R_s), \quad (71)$$

where

$$R_0 = (f_1)^{-3} \left\{ (k')^2(p^2 - s^2) - \frac{4}{3} k'(k + \gamma)(p^3 - s^3) \right.$$  

$$+ \frac{1}{2} \left[ (k')^2 + 4k'\gamma + \gamma^2](p^4 - s^4) - \frac{4}{5} (k'\gamma + \gamma^2)(p^5 - s^5) + \frac{\gamma^2}{3} (p^6 - s^6) \right\}, \quad (72)$$

$$R_s = \delta(1 - p)^3(f_1)^{-3} \left[ -2(k' - \gamma)^2 \left( p - s + \ln \frac{1 - p}{1 - s} \right) \right.$$  

$$+ (2k'\gamma - \gamma^2)(p^2 - s^2) - \frac{2}{3} \gamma^2(p^3 - s^3) \right]. \quad (73)$$
For an asymmetric transistor the numerical factor of 64 should be changed to 16 and the $g_0$ appropriate for a one-sided device must be used.

In the limit $L_1 \to L$, the portion of $|i_{g1}^2|$ proportional to $R_0$ is identical to the expression obtained by van der Ziel (1963a); furthermore, the term proportional to $R_\delta$ represents the hot electron contribution obtained by Baechtold (1972).

2. Short-Circuit Gate Current Fluctuations Produced by Sources in Region II

The fluctuating charges induced on the gate by the noise sources in region II stem from the channel height modulation in regions I and II produced by the fluctuating channel current generated by the dipoles under short-circuit drain conditions. The charge induced by the dipoles on the gate segment adjacent to region I, which we denote as $q_{21}$ is given by

$$q_{21} = -2qNZ \int_0^{L_1} \Delta b(x) \, dx \quad (74a)$$

$$= -2qNZi_{d2} \int_0^{L_1} \frac{db}{dl_d} \, dx. \quad (74b)$$

With the identity $db/dl_d = -adw/dl_d$, and the relation

$$I_d x = g_0ZW_{00} f_1(s, w)$$

obtained from Eq. (7), one may express the integral in terms of the reduced potential, $w(x)$. Integrating over the range $s \leq w \leq p$, we obtain

$$q_{21} = -\frac{2aqNZL_1 k'(y = 0)}{I_d} i_{d2}. \quad (75)$$

The charge induced on the gate in region II is simply

$$q_{22} = -(L_2/v_s)i_{d2}. \quad (76)$$

Combining $q_{21}$ and $q_{22}$, the total induced gate charge produced by the dipoles is

$$q_2 = q_{21} + q_{22}$$

$$= -\frac{2aqNZL_1 k'(y = 0)}{I_d r_d} v_{d2}. \quad (77)$$

Taking the mean square value and multiplying by $\omega^2$, we obtain the short-circuit gate current $|i_{g2}^2|$,

$$|i_{g2}^2| = \omega^2 I_d \frac{16a^3 qD\Delta f^2}{\pi^5 v_s^5} \left[ \frac{L_1 k'(y = 0)}{\kappa e_0 b_p Z(1 - p)r_d} \right]^2 \sin^2 \frac{\pi b_p}{2a}$$

$$\times \left( \exp \frac{\pi L_2}{a} - 4 \exp \frac{\pi L_2}{2a} + 3 + \frac{\pi L_2}{a} \right). \quad (78)$$
This equation also applies to the asymmetric transistor provided the factor 16 is changed to 64 and the $I_d$ and $r_d$ apply to the one-sided transistor.

D. The Correlation Coefficient

Some correlation must exist between the short-circuit gate and drain noise currents since the elementary noise voltages in the channel are responsible for both. Using $i_g = i_{g1} + i_{g2}$ and $i_d = i_{d1} + i_{d2}$ in the expression for the correlation coefficient, Eq. (45) and recognizing that the pairs $(i_{g1}, i_{d2})$ and $(i_{g2}, i_{d1})$ are uncorrelated because they arise from uncorrelated sources, one may conveniently express the correlation coefficient $jC$ as the sum of two terms, $JC_1$ and $JC_2$, corresponding to regions I and II, respectively, where

$$jC_1 = JC_{11} \left( \frac{i_{g1}^2}{i_g^2} \left| i_{d1}^2 \right| \right)^{1/2} \quad \text{and} \quad jC_2 = JC_{22} \left( \frac{i_{g2}^2}{i_g^2} \left| i_{d2}^2 \right| \right)^{1/2}$$

(79)

with

$$JC_{11} = \frac{i_{g1}^2 i_{d1}}{\left( i_{g1}^2 \left| i_{d1}^2 \right| \right)^{1/2}} \quad \text{and} \quad JC_{22} = \frac{i_{g2}^2 i_{d2}}{\left( i_{g2}^2 \left| i_{d2}^2 \right| \right)^{1/2}}.$$  

(80)

Here $JC_{11}$ and $JC_{22}$, respectively, are the "self" correlation coefficients applicable to regions I and II. Except for the different boundary conditions and the inclusion of a field-dependent temperature, the derivation of $C_{11}$ coincides with the treatment of van der Ziel (1963a) for the nonsaturating transistor. It can be shown (Statz et al., 1974) that

$$C_{11} = \frac{S_0 + S_\delta}{\left[(R_0 + R_\delta)(P_0 + P_\delta)\right]^{1/2}},$$

(81)

where

$$S_0 = (f_1)^{-2} \left[ k' [(p^2 - s^2) - \frac{4}{3}(p^3 - s^3) + \frac{1}{2}(p^4 - s^4)] + \gamma \left[ -\frac{3}{4}(p^3 - s^3) + (p^4 - s^4) - \frac{3}{4}(p^5 - s^5) \right] \right]$$

(82)

and

$$S_\delta = 2\delta (f_1^{-2})(1 - p)^3 \left[ (k' - \gamma) \left( s - p + \ln \frac{1 - s}{1 - p} \right) + \frac{1}{2} \gamma (p^2 - s^2) \right].$$

(83)

For no electron heating, $S_\delta = 0$. If in addition there is no velocity saturation so that $\gamma = 0$ and $p = d$, then $C_{11}$ coincides with van der Ziel's result.

Turning to $C_{22}$, an inspection of Eq. (77) reveals that $q_2$ is related to $v_{d2}$, hence $i_{d2}$, by a spatially independent factor. Thus $i_{d2}$ and $i_{g2}$ are fully correlated, $i_{g2}^* i_{d2} = j(i_{g2}^2 \left| i_{d2}^2 \right|)^{1/2}$. Hence $C_{22} = 1.$
E. Noise Coefficients

We shall now define a set of dimensionless noise coefficients based on the preceding analysis which are convenient for noise figure calculations. Let

\[ P = \frac{\overline{i_d^2}}{4kT_o \Delta f g_m} \]  
\[ = P_1 + P_2 \]  
(84a)

and

\[ R = \frac{\overline{i_g^2}}{4kT_o \Delta f \omega^2 C_{sg}^2 / g_m} \]  
\[ = R_1 + R_2 \]  
(85a)

where \( P_1, P_2 \) and \( R_1, R_2 \) are of the same form as \( P \) and \( R \), respectively, but with the subscripts (1) and (2) attached to \( i_d \) and \( i_g \). Thus the subscripts on the \( P \) and \( R \) coefficients refer to regions I and II.

In terms of these coefficients the algebraic factor in the correlation coefficient takes the form

\[ C = \frac{S_0 + S_\delta}{(R_0 + R_\delta)(P_0 + P_\delta)} \sqrt{P_1 R_1 \over PR} + \sqrt{P_2 R_2 \over PR} . \]  
(86)

Using (20) for \( g_m \), (25) for \( r_d \), and (31) for \( C_{sr} \), the components of the \( P \) and \( R \) coefficients of the asymmetric transistor are

\[ P_1 = \frac{1 - p}{f_1 f_g \gamma^2} (P_0 + P_\delta) \]  
(87a)

\[ P_2 = \frac{1 - p}{\xi f_1^2 f_g^2 a} f_3 \]  
(87b)

\[ R_1 = 4 \left( \frac{L}{a} \right)^2 \left( \frac{f_1}{1 - p} \right)^3 \left( \frac{1}{\xi \gamma^2} \right)^2 f_g^2 (R_0 + R_\delta) \]  
(87c)

\[ R_2 = 4 \left( \frac{L}{a} \right)^3 \left( \frac{1}{\xi (1 - p)} \right)^3 \frac{f_1 f_g}{f_1^2 f_g^2} [k'(\gamma = 0)]^2 f_3 \]  
(87d)

where

\[ f_3 = \frac{16}{\pi^3} \left( \frac{D}{D_0} \right) \left[ \sin \left( \frac{\pi}{2} (1 - p) \right) \right]^{1/2} \left( \exp \frac{\pi L_2}{a} - 4 \exp \frac{\pi L_2}{2a} + 3 + \frac{\pi L_2}{a} \right) . \]  
(88)

To obtain \( f_3 \) we have used the relation \( D_0 = (kT_0/q)\mu_0 \) for the low-field diffusion constant.
The coefficients $P$ and $R$ are strong functions of the drain current because of the dependence of the dipole noise contribution on this current. Indeed at high drain currents, $I_d/I_s > 0.1$, corresponding to gate bias voltages near zero, the dipole contribution is the dominant one for $L/a$ ratios even as high as 10. This point is illustrated in Fig. 20a where we have plotted the fraction of the total drain and gate noise contributed by region II, that is the ratios $P_2/P$ and $R_2/R$, respectively. Note that for $I_d/I_s > 0.2$, over 75% of the noise is contributed by region II for the long gate device, $L/a = 10$. This is raised to 95% for the short gate design. The predominance of dipole noise is illustrated even more vividly by the correlation coefficient. In Fig. 20b we have plotted the contribution of region II to the total correlation coefficient, that is, the fractional contribution of the second term $jC_2$ in Eq. (79). Note also that the total correlation coefficient, which is also graphed, is near unity.

In the next section we shall make use of the $P$, $R$, and $C$ functions in the derivation of the noise figure of the FET amplifier.

V. Noise Figure

A. Introduction

The validity of our noise theory can be tested only by its application to a practical device for which the necessary design parameter values are known, and for which the parasitic resistances have been measured.

It is not necessary to include all of the equivalent circuit parameters of the FET since some have a small effect on the noise figure. For example, for simplicity we shall neglect the (small) feedback drain-gate capacitance $C_{dg}$ as well as the source-drain capacitance $C_{sd}$, Fig. 11. The small perturbation of the noise figure produced by these capacitances can be added later if necessary (Klaassen and Prins, 1969; Dahlke, 1955; Hartmann and Strutt, 1973). We may also neglect the small effect of the output drain resistance $r_d$ because the product $g_m r_d \ll 1$ (van der Ziel, 1962). Finally, any small source-lead inductance attributable, for example, to wire bonds, will not be considered. This inductance, whose effect on the noise figure also may be added later, can actually improve (lower) the noise figure slightly (Anastassiou and Strutt, 1974).

The equivalent circuit of the FET to be used in our noise figure analysis is shown in Fig. 21. This was derived from the circuit of Fig. 11 by setting $C_{dg}$, $C_{sd}$, and $g_d = r_d^{-1}$ to zero. Notice that no noise generator is shown with the intrinsic depletion layer charging resistance $R_i$. The noise associated with $R_i$ is imbedded in the gate noise generator $i_g$. This has been demonstrated theoretically by van der Ziel and Ero (1964) and later verified
FIG. 20. Fraction of the total intrinsic noise of the GaAs FET attributable to the diffusion noise of Region II. Shown are gate and drain noise and the correlation coefficient as a function of the normalized drain current for several values of the geometric ratio $L/a$. $V_{sd}/W_{00} = 1$, $\xi = 0.1$. (a) Gate and drain noise, (b) correlation coefficient.
experimentally by Bruncke and van der Ziel (1966). The trans-admittance \( y_m \) representing the current generator of the intrinsic transistor can be approximated by the form \( y_m = g_m e^{-j\omega \tau} \) where \( \omega \tau \) is a phase shift produced by the transit time \( \tau \) of the electrons in the channel (Wolf, 1970; Liechti et al., 1972). Since we have neglected transit time effects in our small-signal and noise analysis, to be consistent we shall also neglect them here.

The intrinsic transistor in its simplified form can be represented by two short-circuit \( Y \) parameters, namely \( Y_{11} \) the input admittance, and \( Y_{21} \) the input-to-output transfer admittance. In terms of the equivalent circuit parameters these can be written as

\[
Y_{11} = j\omega C_{sg}/(1 + j\omega C_{sg} R_i) \tag{89a}
\]

\[
Y_{21} = g_m/(1 + j\omega C_{sg} R_i) \tag{89b}
\]

where, in the expression for \( Y_{21} \), we have set \( y_m = g_m \).

**B. Noise Figure Derivation**

The configuration shown in Fig. 21 with the source-terminal common to input and output is often called the grounded-source or common-source connection. Although we shall derive the expression for the noise figure for this circuit, our results will also apply with negligible error to the common-gate and common-drain configurations (van der Ziel, 1969; Kässer, 1972).
The noise figure $F$ can be expressed in the form

$$F = 1 + \frac{|i_{m0} + i_{g0} + i_{d0}|^2}{|i_{s0}|^2}$$  \hspace{1cm}(90)$$

where $i_{m0}$, $i_{g0}$, $i_{d0}$, and $i_{s0}$ are the noise current components in the short-circuited drain-source path produced by the noise generators $e_m$, $e_i$, $i_g$, $i_d$, and $e_s$, respectively. The noise generators representing the extrinsic thermal sources are given by their mean square values, $\langle e_m^2 \rangle = 4kT_0 R_m \Delta f$, $\langle e_i^2 \rangle = 4kT_0 R_i \Delta f$, and $\langle e_s^2 \rangle = 4kT_0 R_s \Delta f$, where $R_s$ denotes the real part of $Z_s$ and $T_0 = 300^\circ$K.

By a straightforward circuit analysis Eq. (90) becomes

$$F = 1 + \frac{1}{R_s} \left| R_m + R_f + |Z_t|^2 \frac{|i_g|^2}{4kT_0 \Delta f} + \left| \frac{1 + Y_{11} Z_t}{Y_{21}} \right|^2 \frac{|i_d|^2}{4kT_0 \Delta f} \right. - \left. 2 \text{Re} \left[ \frac{Y_{11}}{Y_{21}} \left( 1 + \frac{1 + Y_{11} Z_t}{Y_{21}} \right)^* \frac{i_g i_d}{4kT_0 \Delta f} \right] \right|$$  \hspace{1cm}(91)$$

where $Z_t = Z_s + R_m + R_f = R_s + R_m + R_f + jX_s$, and “Re” denotes the “real part of.” The first two contributions, embodied in $R_m$ and $R_f$, represent the thermal noise of the gate and source parasitic resistances. The third and fourth contributions refer to the induced gate current and the drain current noise of the intrinsic transistor and the last term the correlation between these two currents, modified by the extrinsic elements $Z_s$, $R_m$, and $R_f$.

It is convenient at this point to represent the intrinsic current sources $i_g$ and $i_d$ in terms of noise conductances $g_{gn}$ and $g_{dn}$, respectively, where

$$g_{gn} = \frac{|i_g|^2}{4kT_0 \Delta f} = (\omega^2 C_{sg}/g_m)R$$  \hspace{1cm}(92a)$$

$$g_{dn} = \frac{|i_d|^2}{4kT_0 \Delta f} = g_m P.$$  \hspace{1cm}(92b)$$

Then by a suitable reorganization of terms the expression for $F$ can be put in the useful form

$$F = 1 + (1/R_s) (r_n + g_n |Z_s + Z_c|^2)$$  \hspace{1cm}(93)$$

where $r_n$ and $g_n$ are the so-called noise resistance and noise conductance, respectively, and $Z_c$ is the correlation impedance (Rothe and Dahlke, 1956).

The expressions for $r_n$, $g_n$, and $Z_c$ can be written in the form

$$g_n = \left| \frac{Y_{11}}{Y_{21}} (g_{dn})^{1/2} - jC(g_{gn})^{1/2} \right|^2 + (1 - C^2)g_{gn}$$  \hspace{1cm}(94a)$$

$$r_n = R_m + R_f + \frac{g_{dn}}{Y_{21}^2} \frac{(1 - C^2)g_{gn}}{g_n}$$  \hspace{1cm}(94b)$$

$$Z_c = R_m + R_f + \frac{1}{g_n} \left( \frac{g_{dn} Y_{11}^*}{Y_{21}^2} + \frac{jC(g_{gn} g_{dn})^{1/2}}{Y_{21}^2} \right).$$  \hspace{1cm}(94c)$$
In terms of $r_n$, $g_n$, and $Z_c$, all the noise properties of the FET with parasitics are embodied in a very simple noisy network, shown in Fig. 22 which precedes the FET (now considered noise-free). Thus $r_n$ represents a thermal voltage generator at the standard temperature $T_0$, $g_n$ a shunt thermal current generator at the same temperature, and $Z_c$ an impedance at absolute zero. The noise figure of this combined network is the same as that of the original noisy FET.

The parasitic resistances $R_m$ and $R_f$ appear as a series combination in both the equivalent noise resistance $r_n$ and the correlation impedance $Z_c$, but not in the equivalent noise conductance $g_n$. One may show that the noise contributions of the parasitics enter in $r_n$, whereas the resistive properties of $R_m$ and $R_f$ are relevant in $Z_c$. In other words, at Kelvin temperatures other than the standard temperature, $T \neq T_0 = 300^\circ K$, the sum $R_m + R_f$ in $r_n$ should be multiplied by the ratio $T/T_0$. If we insert the expressions for $g_{gn}$ and $g_{dn}$ in terms of the noise functions $R$ and $P$, Eq. (92), the expressions for $r_n$, $g_n$, and $Z_c$ take on a particularly simple form,

$$r_n = (R_m + R_f) + K_r \left(1 + \frac{\omega^2 C_{sg}^2 R_i}{g_m}\right)$$  \hspace{1cm} (95a)

$$g_n = K_s \frac{\omega^2 C_{sg}^2}{g_m}$$  \hspace{1cm} (95b)

$$Z_c = (R_m + R_f) + \frac{K_c}{Y_{11}}$$  \hspace{1cm} (95c)

where $K_s$, $K_c$, and $K_r$ are functions of $P$, $R$, and $C$. We shall consider these
$K$ functions as our fundamental noise coefficients. They are given by the rather complicated forms,

$$K_g = P[(1 - C(R/P)^{1/2})^2 + (1 - C^2)R/P]$$  \hfill (96a)

$$K_c = \frac{1 - C(R/P)^{1/2}}{(1 - C(R/P)^{1/2})^2 + (1 - C^2)R/P}$$  \hfill (96b)

$$K_r = \frac{R(1 - C^2)}{(1 - C(R/P)^{1/2})^2 + (1 - C^2)R/P}.$$  \hfill (96c)

These coefficients are plotted as a function of normalized drain current in Figs. 23a,b,c for three different $L/a$ ratios and saturation indices $\xi$, typical of practical devices. The coefficient values for other design parameter values can be obtained by interpolation. These coefficients are also displayed as functions of the ratio $L/a$ in Fig. 24. To compute these graphs, we have used $\delta = 1.2$ in Eq. (51a) to fit Baechtold’s experimental $T_e(E)$ data (1972) with our choice of $E_s = 2.9$ kV/cm. In addition we have chosen $D = 35$ cm$^2$/sec for the high field diffusion coefficient. This choice was dictated by the best fit between computed and measured noise figures, and will be discussed more fully later.

Notice that of the three coefficients, $K_g$ shows the strongest increase with drain current, reflecting the strong current dependence of the drain noise function $P$. The least dependence on drain current is exhibited by $K_c$, which also is mildly dependent on $L/a$. Observe that whereas $K_r$ and $K_g$ increase strongly with increasing $L/a$, $K_c$ decreases.

The curves illustrated in Figs. 23 and 24 apply for the drain bias condition $V_{sd}/W_{00} = 1$. There is a small drain voltage dependence of these $K$ coefficients. This is illustrated in Fig. 25. Observe, though, that in the range $0.5 < V_{sd}/W_{00} < 1$, which encompasses most practical bias conditions, the variation is small. The variation in the optimum noise figure, as we shall show later, is even less.

It is to be noted that for short gate lengths, when region II encompasses most of the channel and dipole noise dominates so that $C \approx 1$, the noise coefficients simplify drastically. In particular, $K_r$ approaches zero.

### C. Minimum Noise Figure

The first stage of a low-noise amplifier chain is usually designed to have a minimum noise figure. The noise figure is optimized by proper choice of the source impedance $Z_s = R_s + jX_s$. This optimization can be achieved by a suitable impedance matching network between the signal source and the input (gate-source) terminals of the FET. As a function of the source
FIG. 23. Noise coefficients as a function of normalized drain current for various values of the saturation index $\xi$. $V_{dd}/W_{00} = 1$. (a) $L/a = 3$, (b) $L/a = 5$, (c) $L/a = 10$. 
impedance, the noise figure expression Eq. (93) has its minimum value when the reactive component of $Z_s$ is equal in magnitude and opposite in sign to the imaginary part of the correlation impedance $Z_c = R_c + jX_c$, and the real part of $Z_s$ has its optimum value $R_{s,\text{opt}}$. Using Eq. (93), it is easy to show that the components of the optimum source impedance are given by

$$R_{s,\text{opt}} = \left[R_c^2 + (r_n/g_n)^2\right]^{1/2} \quad (97a)$$

$$X_{s,\text{opt}} = -X_c \quad (97b)$$

The minimum value of $F$ can be expressed as

$$F_{\text{min}} = 1 + 2g_n(R_c + R_{s,\text{opt}}) \quad (98a)$$

or in decibels as

$$F_{\text{min}} (\text{dB}) = 10 \log_{10} F_{\text{min}}. \quad (98b)$$
FIG. 25. Noise coefficients as a function of the normalized drain voltage for the case \( L/a = 5 \). The drain current is held fixed. \( I_d/I_s = 0.5, \xi = 0.1 \).

It shall be helpful for later discussions to expand the rather complicated appearing frequency dependence of \( F_{\text{min}} \) in a power series in \( \omega \). By straightforward algebra, we obtain

\[
F_{\text{min}} = 1 + 2(\omega C_{sg}/g_m)[K_g[K_r + g_m(R_m + R_f)]^{1/2} + 2(\omega C_{sg}/g_m)^2[K_g g_m(R_m + R_f + K_c R_i)] + \cdots .
\]

The appearance of \( g_m \) and the parasitic resistances in the linear frequency term emphasizes the dominant role played by these parameters in the optimum noise performance of an FET. Notice that \( R_i \) appears in the quadratic term only.

The ratio \( \omega C_{sg}/g_m \) appearing in this expansion can be expressed as \( f/f_r \), where \( f_r = g_m/2\pi C_{sg} \) is the gain-bandwidth product of the FET. It is also the frequency at which the current gain of the FET drops to unity. FETs usually are not operated at frequencies above \( f_r \) because of the severe degradation in power gain as \( f_r \) is exceeded.

VI. EXPERIMENTAL DATA

A. Introduction

We have applied our small-signal and noise theory to a practical \( n \)-type GaAs FET whose published design values stated by Brehm (1973) and Brehm and Vendelin (1974) are as follows: \( L = 2 \mu m, a = 0.2 \mu m, \)
Z = 2.85 \times 10^{-2} \text{ cm}, N_d = 10^{17} \text{ cm}^{-3}, \text{ and } W_{00} = 2.9 \text{ V}. The values of the parasitic resistances are R_T = 15 \Omega \text{ and } R_m = 0.8 \Omega. This design closely parallels geometries studied at various laboratories including our own at the Research Division of the Raytheon Company.

The noise coefficients and small-signal parameters were calculated by us by first solving for the internal parameters s and p as a function of the bias voltages. A computer program based on the equations of Sections II and III was written for this purpose. As a by-product we also obtained the solutions for the $I$-$V$ characteristics. As a spot check of our dc and small-signal theory, we compute for a zero gate bias and a 3 V drain bias, a saturation drain current $I_{dss} = 28.3 \text{ mA}^*$ and a terminal conductance $g_{m}^* = 19 \text{ mmho}$, both values within 5% of Brehm and Vendelin's experimental data (1974). We also have made similar calculations for our own device designs, and obtained equally good agreement with experiment.

It might be of interest to point out that for this device design our computer results show that for the drain-source bias corresponding to current saturation, i.e., above the "knee" of the $I_d$-$V_{dd}$ curves, the length of the saturated velocity region is of the order of 30% of the gate length $L$. (For shorter gate lengths, of the order of 1 $\mu$m, this fraction can be as high as 90%.) The computed channel opening for the bias conditions stated above is almost uniform along the entire length of the gate, $s \approx 0.68$, $p \approx 0.76$. Thus, the longitudinal voltage drop along the channel in region I is negligible compared to the corresponding drop in region II.

The noise figure calculation requires a value for the gate charging resistance $R_g$. Since there is at present no analytic formula for $R_g$ for the two-region channel model, we have assumed that the $R_g C_{sg}$ product is approximately proportional to the transit time $\tau$ through the channel, where

$$\tau = \int_0^L \frac{dx}{v(x)} = \int_0^{L_1} \frac{dx}{\mu_0 E(x)} + \int_{L_1}^L \frac{dx}{v_s}. \quad (100)$$

There are sound theoretical grounds for this assumption, since in the constant mobility case, i.e., $L_1 = L$, $R_g C_{sg}$ is proportional to $\tau$ (Hower et al. 1969, 1971). In this case $\tau$ is strongly dependent on bias conditions of course. When velocity saturation is present, the transit time calculated from (100) is very nearly equal to the constant value $L/v_s$, as if region II extended over the entire gate length!

Using the values of $R_g$ and $C_{sg}$ derived from the experimental data of Brehm and Vendelin (1974), we set $R_g C_{sg} = 4 \times 10^{-12} \text{ sec}$. In passing we note that this product seems to scale with gate length, so that for a gate

*$I_{dss}$, the saturation drain current at zero gate bias, should not be confused with $I_s$, the normalizing saturation current used earlier.
length $L = 0.9 \mu m$, this product is $\sim 1.8 \times 10^{-12}$ sec (Liechti et al., 1972). In any case, a precise value for $R_i$ is not important, since it appears in the second-order term of the power series expansion for $F_{\text{min}}$, Eq. (99).

B. Experimental Results

As a preliminary to our noise figure presentation, we illustrate in Fig. 26 the calculated dependence of the noise conductances $g_{ga}$ and $g_{dn}$ on the gate bias or more precisely on the normalized drain current $I_d/I_{dss}$ (see footnote

![Figure 26](image)

**Fig. 26.** Equivalent gate noise conductance $g_{gn}$, drain noise conductance $g_{dn}$, and correlation coefficient magnitude as a function of drain current for a specified value of the high field diffusion constant $D$. The design parameters for the FET are: $L = 2.0 \mu m$, $a = 0.2 \mu m$, $Z = 285 \mu m$, and $N = 10^{17} \text{cm}^{-3}$. 

*Note: The figure shows the relationship between $D = 35 \text{cm}^2/\text{sec}$, $V_{dd} = 3.0 \text{V}$, and $f = 4.0 \text{GHz}$.*
p. 253) for a particular value of the high field diffusion constant, $D$. For other values of $D$ our computations show that these conductances are nearly proportional to $D$ except at the low end of the drain current scale. This illustrates the predominance of the high field dipole noise of region II. This is further emphasized by the near unity correlation coefficient displayed in this graph.

Figure 27 illustrates the dependence of $F_{\text{min}}$ on the normalized drain current for a particular value of drain bias and several values of the high field diffusion constant. Also shown are the experimental results for the two devices reported by Brehm and Vendelin (1974). It is evident that the choice

![Figure 27. Comparison between theoretical and experimental noise figures for a microwave GaAs FET as a function of drain current. The solid curve labeled $D = 35 \text{ cm}^2/\text{sec}$ is the best fit to the experimental data. Shown also are theoretical curves for values of the high field diffusion coefficient above and below the value giving the best fit. The rapid increase of $F_{\text{min}}$ with drain current is caused by the diffusion noise of the velocity-saturated region. This is made evident by the curve labeled $D = 0$ which corresponds to no diffusion noise. The upturn in noise figure to the left of the minimum is caused by the rapid decrease of $g_m$ at low currents. The curve labeled $R_m + R_f = 0$ represents the intrinsic noise of the FET. +, ●, Experiment (Brehm and Vendelin, 1974); —, − − −, theory. (Experimental data, Brehm and Vendelin, 1974, courtesy of Microwaves.)](image-url)
$D = 35 \text{ cm}^2/\text{sec}$ provides the best fit to the experimental data. This value is substantially lower than the low-field number $D_0 = kT_0 \mu_0/q = 110 \text{ cm}^2/\text{sec}$, and the high-field values measured by Ruch and Kino (1968). However, it is in good agreement with the experimental high-field values reported recently by Castelain et al. (1974), and is in general agreement with the high-field levels computed by Fawcett and Rees (1969). Since the circuit losses were not stated by Brehm and Vendelin, we could not correct the measured noise figure for them. We may speculate that these losses could increase the noise figure by approximately 0.25–0.5 dB, so that the choice of $D$ might have to be revised downward. Obviously more experimental data are necessary to resolve this uncertainty.

Notice that our theoretical results exhibit all of the features of the experimental data, in particular the rapid rise of $F_{\text{min}}$ at high drain currents, a property not shared by other noise theories. This rapid rise in $F_{\text{min}}$ at high drain currents and the strong dependence on the diffusion constant is a measure of the strong influence of the diffusion noise of region II. This dependence is embodied primarily in the noise coefficient $K_k$. To further demonstrate the dependence on $D$, we also have plotted in Fig. 27 the curve for $D = 0$, that is, for no dipole noise. Note that $F_{\text{min}}$ no longer increases with drain current, but actually decreases!

The degradation of the noise figure to the left of the minimum, on the other hand, is a consequence of the sharp drop-off of $g_m$ at extremely low currents, as is evident from Eq. (99). Because of this, the width of the trough in the $F_{\text{min}}$ curve can be quite broad if the decrease in $g_m$ extends over an extended current region. This would occur, for example, if the doping profile at the substrate interface were not sharp but tapered off slowly as the interface is approached.

We also show in Fig. 27 the value of $F_{\text{min}}$ in the absence of parasitics ($R_m = R_f = 0$). The low level of $F_{\text{min}}$ derives from the strong cancellation of noise due to correlation, as predicted by the expression for $F_{\text{min}}$ which for this case simplifies to

$$F_{\text{min}} = 1 + (2\omega C_{ss}/g_m)[PR(1 - C^2)]^{1/2} + \cdots$$

(101)

where the factor $(1 - C^2)$ is very small. The effectiveness of the noise cancellation produced by correlation is diminished drastically when the parasitic elements are introduced. It is obvious then that parasitic resistances should be kept to a minimum, not only because they introduce noise of their own, but also because they indirectly cause an increase in the contributions of the noise sources associated with the intrinsic device.

The importance of maintaining low parasitic resistances is illustrated further in Fig. 28. This is a graph of the predicted minimum noise figure as a function of parasitic resistance. Note the considerable degradation in noise figure as $(R_m + R_f)$ exceeds the design value.
When the device is biased well above the knee of the $I-V$ characteristic, that is, in the current saturation regime, the minimum noise figure is a mild function of the drain bias voltage. This is illustrated by the experimental results of Brehm (1973) and Brehm and Vendelin (1974) shown in Fig. 29. Note the excellent agreement between their data and our theoretical results.

It is informative to predict the minimum noise figure for frequencies other than 4 GHz. Figure 30 is a graph of $F_{\text{min}}$ for the frequency range extending from 1 to 10 GHz. This graph was computed with the exact expression for $F_{\text{min}}$, Eq. (98). Note the nearly linear dependence on frequency.

Figure 31 shows how the noise figure varies with gate length. Note the significant reduction in $F_{\text{min}}$ for a 1 µm gate. The predicted noise figure for the shorter gate lengths are substantially lower than the results reported in the literature (Liechti et al., 1972) for 10 GHz operation. This disagreement may indicate some limitations in the validity of our analysis for these short gate lengths, since the gradual channel approximation in region I may no longer be valid. Only more experimental data can resolve this question.

It is possible, however, that the experimental noise figures reported to date for X band are higher than predicted because of other reasons. First, circuit losses neglected in our computations become increasingly important at the higher microwave frequencies and may possibly explain some of the discrepancy. Second, processing techniques for the shorter gate lengths are
not as well developed as for the longer gate lengths, so that the practical device may not be represented accurately enough by the simple equivalent circuit used in our analysis. Third, trap noise originating in the epitaxial layer, or more likely at the interface between the epitaxial layer and the substrate, may be significant.

There is some experimental evidence that trap-related noise may be important at microwave frequencies. For example, experiments performed by the authors have demonstrated that sources at the epitaxial substrate interface, presumably traps, can generate drain current noise whose spectrum extends from below the video band (30 MHz) up through C band. Luxton (1973) of the Plessey laboratories reports that the growth of a high resistivity epitaxial buffer layer between the substrate and the channel layer improves the noise figure of microwave frequencies. This may indicate that the buffer layer reduces the effectiveness of short lifetime interface traps.

Noise originating from short lifetime traps may also explain the higher than theoretical noise figure observed at the low end of the microwave band.
FIG. 30. Theoretical minimum noise figure as a function of frequency for the device design considered in the text. $L = 2.0 \, \mu m$, $a = 0.2 \, \mu m$, $Z = 285 \, \mu m$, $N_d = 10^{17} \, cm^{-3}$, $V_{dd} = 3.0 \, V$.

FIG. 31. Predicted minimum noise figure as a function of gate length for the device design considered in the text. $a = 0.2 \, \mu m$, $Z = 285 \, \mu m$, $N_d = 10^{17} \, cm^{-3}$, $V_{dd} = 3.0 \, V$. 
extending from 0.5 to 3 GHz. The observed noise figure in this band does not continue to decrease with frequency at the nearly linear rate exhibited by the graph in Fig. 30; rather it decreases at a much slower rate (Baechtold et al., 1973; Luxton, 1974).

The linear frequency variation at small $\omega$ originates from the quadratic frequency dependence of the gate noise $|i_{gn}^2|$. [One may show this by expressing $R$ in Eq. (101) in terms of the gate noise generator using Eq. (92a).] Now, single-level traps introduce a noise component in the drain current varying with frequency as

$$\frac{|i_{g}^2|}{\sim K/(1 + \omega^2 T^2)}$$

(102)

(van der Ziel, 1963b; Halladay and Bruncke, 1963; Copeland, 1971), where $K$ is a constant of the device and the traps. The induced gate noise, consequently, will have a component of the form

$$\frac{|i_{g}^2|}{\sim K'\omega^2/(1 + \omega^2 T^2)}$$

(103)

(Jordan and Jordan, 1965). At frequencies substantially higher than the inverse trap lifetime, $\omega \gg T^{-1}$, this gate-current component will become frequency independent. Thus, presumably, in the low microwave band the total gate noise current can be approximated by the expression

$$\frac{|i_{g}^2|}{\sim A + Bo^2}$$

(104)

where the constant term is produced by traps. Thus $F_{min}$ would decrease at a slower than linear frequency rate when the second term became comparable to the first.

There is obviously a need for further research on the role of traps in microwave FETs, but it appears hopeful that improved technology for the growth of epitaxial layers, including high resistivity buffer layers, will reduce the noise contributed by traps.

**C. Summary and Conclusion**

We have shown that the saturated velocity region plays a significant role in determining the small-signal and noise properties of GaAs microwave FETs. The theory presented here differs in several important respects from previous theories. First, the extent of the velocity-saturated regime is not restricted to the very edge of the channel as Turner and Wilson (1969) and Baechtold (1972) have assumed, but is allowed to extend into the channel a significant distance from the drain end, depending on the bias conditions. A consequence of this is that a finite drain resistance is predicted. Second, because of the nonzero extent of the saturated velocity region, a new noise generating mechanism is introduced.
We have shown for microwave designs that the noise produced in the velocity-saturated region increases with the dc level of drain current, and explains the experimental dependence of the noise figure on this current. At the higher drain currents, this noise predominates.

We have presented an extensive series of curves for the small-signal and noise parameters. These are given in a form suitable for the device engineer to predict the performance of a particular design.

While we have demonstrated good agreement between our theory and some limited experimental results, it is still too early to establish the limits of validity of this theory until more extensive experimental data becomes available for a wider range of design parameters.

APPENDIX I: DERIVATION OF GATE CAPACITANCE EXPRESSION

We derive the expression for the field-component normal to the surface of the gate electrode, i.e., \( E_x(x, a) \), then integrate it over the surface to obtain the total gate charge, \( Q_g \). The gate capacitance is the derivative of \( Q_g \) with respect to gate bias.

The \( y \) component of field consists of two parts, \( E_{y1}(x, a) \) in region I, and \( E_{y2}(x, a) \) in region II. In region I the field is simply that produced by the ionized impurities of the depletion region. Thus

\[
E_{y1}(x, a) = (2W_{00}/a)[1 - b(x)/a].
\]

In region II there is an additional component produced by the Laplacian potential Eq. (17), so that

\[
E_{y2}(x, a) = (2W_{00}/a)p + E_s \sinh \left[ \pi(x - L_1)/2a \right]
\]

where \( p = 1 - b_p/a \).

Integrating this field over both gate electrode areas, one obtains the total gate charge \( Q_g \),

\[
Q_g = 2\kappa e_0 Z \left[ \int_0^{L_1} E_{y1}(x, a) \, dx + \int_{L_1}^L E_{y2}(x, a) \, dx \right].
\]

which after some manipulation, becomes

\[
Q_g = 2qNaZ \left[ \frac{f_2(s, p)}{f_1(s, p)} L_1 + \frac{\xi a^2}{\pi L} \left( \cosh \frac{\pi L_2}{2a} - 1 \right) \right]
\]

where \( f_2(s, p) \) is given by Eq. (30). Performing the differentiation \( C_{gg} = dQ_g/dV_{sg} \), holding \( V_{sd} \) constant and using the identity

\[
\frac{dp}{dV_{sg}} \bigg|_{V_{sd}} = \frac{f_g}{W_{00}}
\]
from Eqs. (19b) and (20), and the relation

\[
\frac{dL_2}{dV_{sg}} \bigg|_{\nu_{ad}} = \frac{1 - 2pf_g}{E_s \cosh (\pi L_2/2a)},
\]

(108b)

obtained by differentiation of (18), we obtain for \(C_{gg}\)

\[
C_{gg} = 2ke_0 Z[f_{c1}(s, p, \xi) + f_{c2}(s, p, \xi) + 1.56]
\]

(109)

where \(f_{c1}(s, p, \xi)\) and \(f_{c2}(s, p, \xi)\) are given by Eq. (32), and the constant term has been added to account for fringing.

Assuming that the feedback capacitance \(C_{dg}\) is small compared to \(C_{gg}\), as experimental data shows, we may write

\[
C_{sg} = C_{gg} - C_{dg} \approx C_{gg}
\]

(110)

so that (109) can be considered an approximation for \(C_{sg}\). This is the expression (31) given in the text.

**APPENDIX II: DERIVATION OF \(|\Delta v_1^2|\)**

We derive in this appendix the open-circuit noise voltage \(\Delta v_1\), and its mean square value \(\sqrt{\Delta v_1^2}\), developed across region I by an elementary thermal noise voltage \(\Delta W_{x_0}\) at some point \(x_0\) in region I.

The noise disturbance will cause a perturbation in the channel height \(2b\) and in the channel field \(dW/dx\) such that the total current \(I_d\) is constant. Let \(\delta W\) be the disturbance in the channel potential \(W\) at some \(x > x_0\); then

\[
\delta I_d = \delta \left(2\sigma b \frac{dW}{dx}\right) = 0,
\]

(111)

which leads to the relation

\[
b \frac{d(\delta W)}{dx} + \frac{dW}{dx} \delta b = 0
\]

(112)

or

\[
\frac{d(\delta W)}{dx} = -\frac{1}{b} \frac{dW}{dx} \delta b
\]

(113)

for the perturbation in the field. The channel width perturbation \(\delta b\) can be eliminated by subjecting the relation

\[
2b = 2a[1 - (W/W_{00})^{1/2}]
\]

(114)

to a perturbation. This yields

\[
\delta b = -\frac{a}{2} (W_{00} W)^{1/2} \delta W.
\]

(115)
Substitution of (115) into (113) gives

$$\frac{1}{\delta W} \frac{d(\delta W)}{dx} = a \frac{1}{2b\left(W_{00}W\right)^{1/2}} \frac{dW}{dx}.$$  \hspace{1cm} (116)

Using (114) for \( b \), and \( W = w^2W_{00} \), we may cast (116) into the form

$$\frac{1}{\delta W} \frac{d(\delta W)}{dx} = \frac{dw}{1 - w}.$$  \hspace{1cm} (117)

We integrate (117) from \( x_0 \) to \( L_1 \), using the definitions \( \delta W(x_0) = \Delta W_{x_0} \), \( \delta W(L_1) = \Delta v_1 \). Thus

$$\Delta v_1 = -\frac{1 - w(x_0)}{1 - p} \Delta W_{x_0}.$$  \hspace{1cm} (118)

Taking the mean square value,

$$|\Delta v_1^2| = \left(\frac{1 - w(x_0)}{1 - p}\right)^2 |\Delta W_{x_0}^2|.$$  \hspace{1cm} (119)

The mean square value of the elementary noise voltage can be expressed in terms of the channel resistance of an elementary section of length \( dx_0 \) at \( x_0 \).

Thus

$$\left|\Delta W_{x_0}^2\right| = 4kT_e(x_0) \Delta f(dW_0W_{00}w/2\sigma_b(x_0)Z)$$  \hspace{1cm} (120)

where \( T_e(x_0) \) is the elevated electron temperature at \( x_0 \). Using the identities

$$E(x_0) dx_0 = dW = 2W_{00}w dw$$  \hspace{1cm} (121)

$$I_d = 2\sigma_b(x_0)ZE(x_0)$$  \hspace{1cm} (122)

in (120) we obtain

$$\left|\Delta W_{x_0}^2\right| = \frac{8kT_e(x_0)W_{00} \Delta f}{I_d} w dw.$$  \hspace{1cm} (123)

Inserting this expression into (119), we finally get Eq. (50) of the text,

$$\left|\Delta v_1^2\right| = \frac{8kT_e(x) \Delta fW_{00}}{I_d(1 - p)^2} (1 - w)^2 w dw.$$  \hspace{1cm} (124)

where \( x_0 = x \) is any point in region I.

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REFERENCES
