A New Approach to Determine the Effective Channel Length and the Drain-and-Source Series Resistance of Miniatursized MOSFET's

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Abstract—A new decoupled C-V method is proposed to determine the intrinsic (effective) channel region and extrinsic overlap region for miniaturized MOSFET's. In this approach, a unique channel-length-independent extrinsic overlap region is extracted at a critical gate bias, so bias-independent effective channel lengths \( L_{\text{eff}} \) are achieved. Furthermore, the two-dimensional (2D) charge sharing effect is separated from the effective channel region. Based on this \( L_{\text{eff}} \) and the associated bias-dependent channel mobility, \( \mu_{\text{eff}} \), the drain-and-source series resistance \( R_{\text{DS}} \) can be derived from the I-V characteristics for each device individually. For the first time, the assumption or approximation for the extrinsic overlap region for miniaturized MOSFET's is avoided, thus the difficulties and controversy encountered in the conventional I-V method can be solved. The 2D charge sharing effect is incorporated into the bias-dependent \( R_{\text{DS}} \). This bias dependence is closely related to the drain/source doping profile and the channel dopant concentration. The proposed \( L_{\text{eff}} \) and \( R_{\text{DS}} \) extraction method has been verified by an analytical I-V model which shows excellent agreements with the measured I-V characteristics.

I. NOMENCLATURE

- \( C_{\text{ext,ov}} \): Maximum extrinsic overlap capacitance between gate and source/drain regions
- \( C_{\text{ov}} \): Direct overlap capacitance associated with the source/drain metallurgical lateral diffusion length \( L_D \)
- \( C_{\text{ff}} \): Inner fringe capacitance
- \( C_{\text{df}} \): Outer fringe capacitance due to finite poly gate thickness
- \( C_{\text{g(vis)}} \): Maximum gate capacitance per unit area under strong inversion condition
- \( C_{\text{s(vis)}} \): Capacitance per unit area attributed to the space charge in the semiconductor layer under strong inversion condition
- \( I_D \): Measured drain current which is subjected to both intrinsic channel resistance and Drain-and-Source series resistance \( R_{\text{DS}} \)
- \( I_{D0} \): Ideal drain current calculated with zero drain-and-source series resistance

Drain-and-Source series resistance
\[ L_M \]
Device gate length drawn on mask
\[ L_d \]
Physical gate length after polysilicon gate etch, \( L_d = L_M - \Delta L_{\text{AEI}} \)
\[ L_{\text{jj}} \]
Effective channel length defined by source/drain metallurgical junctions
\[ L_D \]
Metallurgical source/drain lateral diffusion length
\[ L_{\text{int, ch}} \]
Intrinsic channel length extracted by the decoupled C-V method
\[ L_{\text{ext,ov}} \]
Extrinsic overlap length extracted by the decoupled C-V method
\[ L_{\text{eff}} \]
Effective channel length used in the I-V model, \( L_{\text{eff}} = L_{\text{int, ch}} \)
\[ \Delta L_{\text{AEI}} \]
Poly silicon gate etch loss
\[ R_{\text{sh}} \]
Sheet resistance (in ohm) of the source/drain diffusion region
\[ R_{\text{sp}} \]
Spreading resistance (in ohm) due to the current crowding from the source/drain diffusion to the channel ends
\[ R_d \]
Sum of sheet resistance and spreading resistance associated with the drain terminal, \( R_d = (R_{\text{sh}} + R_{\text{sp}})_{d} \)
\[ R_s \]
Sum of sheet resistance and spreading resistance associated with the source terminal, \( R_s = (R_{\text{sh}} + R_{\text{sp}})_{s} \)
\[ R_S \]
Total series resistance in the source terminal, \( R_S = R_s + R_C \)
\[ R_D \]
Total series resistance in the drain terminal, \( R_D = R_d + R_C \)
\[ R_C \]
Source/drain contact resistance
\[ R_{\text{DS}} \]
Drain-and-Source series resistance including \( R_D \) and \( R_S \), \( R_{\text{DS}} = R_D + R_S \)
\[ V_T \]
Threshold voltage of the intrinsic channel region
\[ V_{\text{GT}} \]
Gate overdrive (= \( V_{\text{GS}} - V_T \))
\[ V_{\text{int,ov}} \]
Gate bias at which the extrinsic overlap length \( L_{\text{ext,ov}} \) is extracted
\[ \mu_{\text{eff}} \]
Effective mobility of the inversion carriers
\( W \)
Device gate width drawn on mask

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of miniaturized MOSFET's. Therefore, an electrical measurement technique with high efficiency and accuracy is urgently demanded by circuit designers to model and predict the scaled device characteristics and circuit performance. Extensive investigations have been performed on this subject, however, controversy always exists among all the techniques proposed and seems very difficult to be eliminated.

Many publications [1]-[5] have promoted the use of multiple MOSFET resistance measurement for the determination of \( L_{\text{eff}} \) and \( R_{\text{DS}} \). However, in most of them, the MOSFET channel mobility is treated as a constant at a fixed gate bias [1]-[4] for a group of devices with various channel lengths or further simplified as a gate-bias-independent constant [5]. This simplification is not consistent with the reality that the inversion carrier mobility is determined by gate overdrive, \( V_{\text{GT}} = V_{\text{GS}} - V_T \), under varying back bias [6]-[8] which in fact contributes to the inversion carrier density instead of just simply gate bias. Some techniques [9], [10] are proposed to take fixed gate overdrive instead of fixed gate bias to keep the mobility and inversion carrier density constant for each device. In this way, the accuracy is expected to be improved, but the bias dependence of \( R_{\text{DS}} \) is still not taken into account. It is just the difficulty encountered in the conventional I-V approach that channel length loss, \( \Delta L \), and series resistance, \( R_{\text{DS}} \), are needed to be extracted simultaneously and then an assumption of bias-independent \( R_{\text{DS}} \) is generally proposed to derive \( \Delta L \) from linear I-V equation. This assumption is not justified on the fact that \( R_{\text{DS}} \) is bias-dependent and a single intersection is not possible to be found. Several articles have discussed on the accuracy of \( L_{\text{eff}} \) and \( R_{\text{DS}} \) determination [11]-[13] by the I-V approach, and it is concluded improvement is still necessary for achieving an accurate characterization and modeling of the I-V characteristics for submicron MOS devices.

In this paper, we will report a totally different approach from the previous works to determine \( L_{\text{eff}} \) and \( R_{\text{DS}} \). A new decoupled C-V method proposed by Guo et al. [14] was used to determine \( L_{\text{eff}} \), and then bias-dependent \( R_{\text{DS}} \) can be derived from I-V characteristics. The difficulties and controversy encountered in the conventional I-V approach can be eliminated. In Section II, we will present the key process steps for device fabrication briefly. In Section III, the new approach to determine \( L_{\text{eff}} \) and bias-dependent \( R_{\text{DS}} \) will be described in detail. \( L_{\text{eff}} \) and \( R_{\text{DS}} \) achieved by this new approach will be demonstrated and discussed in Section IV. Based on these two parameters, a physically based I-V model has been developed to keep both high accuracy and simplicity. Finally, a conclusion will be summarized.

### III. DEVICE FABRICATION

MOSFET's with single drain (SD) and lightly doped drain (LDD) structures used in this study were fabricated by 0.7 \( \mu m \) poly gate CMOS technology. The gate oxide thickness is 145 \( A \). The single drain (SD) was formed by \( 5 \times 10^{15} \, \text{cm}^{-2} \) 80 Kev As\textsuperscript{+75} implant. The channel implants were split with the doping concentrations from around \( 1 \times 10^{16} \, \text{cm}^{-3} \) to \( 2 \times 10^{18} \, \text{cm}^{-3} \) as listed in Table I. As for the LDD MOSFET, the LDD was first formed by \( 2.5 \times 10^{12} \, \text{cm}^{-2} \) 50 Kev \( P^{+} \) implant, and followed by \( 5 \times 10^{15} \, \text{cm}^{-2} \) 80 Kev As\textsuperscript{+75} implant masked by 0.15 \( \mu m \) oxide spacer. Furthermore, a nonuniform channel doping profile was produced by the \( V_T \) adjust implant plus an anti-punchthrough implant for these LDD N-channel devices.

### IV. A NEW APPROACH TO DETERMINE THE EFFECTIVE CHANNEL LENGTH AND THE DRAIN-AND-SOURCE SERIES RESISTANCE

#### A. Determination of the Effective Channel Length

C-V measurement for the short channel devices (\( W/L_M = 100 \, \mu m (0.7, 0.8, 1.0, \text{and} 1.2 \, \mu m) \)) was performed using high resolution LCR meter HP4284A. The frequency and amplitude of the AC signal are specified at 100 kHz and 100 mV, respectively. Fig. 1(a) shows the measured gate to source/drain capacitance, \( C_{\text{GS}} + C_{\text{GD}} \), from the accumulation to inversion regions and the insert shows the configuration for the measurement. A critical gate bias point \( V_{\text{int, on}} \) is observed in the \( (C_{\text{GS}} + C_{\text{GD}}) - V_{\text{GS}} \) characteristics as a boundary between two distinct regions at which the extrinsic overlap length, \( L_{\text{ext, ov}} \), is determined. Region I is subjected to the gate bias below \( V_{\text{int, on}} \) where the C-V characteristics are independent of the device channel length. Region II is subjected to the gate bias above \( V_{\text{int, on}} \) where the C-V characteristics are strongly dependent on the channel length. The former is considered to be contributed from the extrinsic overlap region and the latter from the intrinsic channel region. The dopant and carrier profiles along the channel surface at \( V_{\text{GS}} = V_{\text{int, on}} \) are investigated by 2D device simulation. The result depicted in Fig. 1(b) shows that the carrier concentration between the extrinsic overlap and intrinsic channel regions just equals to the dopant concentration in the intrinsic channel region. The intrinsic channel and extrinsic overlap lengths, \( L_{\text{int, ch}} \) and \( L_{\text{ext, ov}} \) can be determined as follows. From Fig. 1(b),

\[
L_y = L_{ij} + 2L_D = L_{\text{int, ch}} + 2L_{\text{ext, ov}}
\]

(1)

where \( L_{\text{ext, ov}} \) is the extrinsic overlap length. \( L_y \) is obtained from \( (C_{\text{GS}} + C_{\text{GD}})_{\text{max}} \) and \( C_{g(\text{inv})} \).

\[
L_y = [(C_{\text{GS}} + C_{\text{GD}})_{\text{max}} - 2C_{\text{of}}]/W C_{g(\text{inv})}
\]

(2)

where \( C_{g(\text{inv})} \) is achieved from large device (\( W = L_M = 100 \, \mu m \)) in strong inversion region,

\[
C_{g(\text{inv})} = C_{\text{ox}} C_{g(\text{inv})}/(C_{\text{ox}} + C_{g(\text{inv})}), C_{\text{ox}} = C_s V_{\text{GS} = V_T}
\]

(3)

and \( (C_{\text{GS}} + C_{\text{GD}})_{\text{max}} \) is obtained from Fig. 1(a) for short channel devices in strong inversion region, i.e.,

\[
(C_{\text{GS}} + C_{\text{GD}})_{\text{max}} = (C_{\text{GS}} + C_{\text{GD}}) V_{\text{GS} = V_T}.
\]

(4)

\(L_{\text{ext, ov}}\) can be determined from \( C_{\text{ext, ov}} \) and \( C_{g(\text{inv})} \), i.e.,

\[
2L_{\text{ext, ov}} = C_{\text{ext, ov}}/WC_{g(\text{inv})}
\]

(5)
where \( C_{\text{ext,ov}} \) can be extracted from the measured \((C_{GS} + C_{GD}) - V_{GS}\) as illustrated in Fig. 1(a), i.e.,

\[
C_{\text{ext,ov}} = (C_{GS0} + C_{GDO})_{\text{max}} - 2C_{\text{of}}
\]

and

\[
(C_{GS0} + C_{GDO})_{\text{max}} = (C_{GS0} + C_{GDO})|V_{GS=V_{\text{int,ch}}}.
\]

Here, \((C_{GS0} + C_{GDO})_{\text{max}}\) is the maximum of the overlap capacitance in region I, with the gate biased at \(V_{\text{int,ch}}\) as illustrated in Fig. 1(a). The overlap capacitance in region I is composed of three components as given by

\[
(C_{GS0} + C_{GDO}) = 2(C_{\text{of}} + C_{\text{if}} + C_{\text{df}})
\]

where \( C_{\text{of}} \) is the outer fringe capacitance contributed from the finite thickness of gate electrode. It can be determined from the minimum \((C_{GS0} + C_{GDO})\) in strong accumulation region achieved for LDD devices. \( C_{\text{df}} \) is the inner fringe capacitance contributed from the early inversion layer (inversion prior to that of intrinsic channel region, i.e., with the smaller threshold voltage than that of intrinsic channel region). \( C_{\text{if}} \) reaches the maximum with gate biased at \(V_{\text{int,ch}}\) which is always below \(V_T\) (threshold voltage of intrinsic channel region). \( C_{\text{of}} \) is contributed from the direct overlap region between the poly gate and the SD metallurgical lateral diffusion region with the length of LD.

Once \( L_g \) and \( L_{\text{ext,ov}} \) have been determined from (2) and (5) respectively, the intrinsic channel length \( L_{\text{int,ch}} \) is calculated by (1). \( L_g \), \( L_{\text{ext,ov}} \) and \( L_{\text{int,ch}} \) extracted by decoupled C-V method are listed in Table I. \( L_{\text{int,ch}} \) is distinguished from \( L_D \) by that \( C_{\text{if}} \) includes both \( C_{\text{of}} \) and \( C_{\text{df}}. C_{\text{df}} \) just contributes to the channel-doping-dependence observed on \( L_{\text{ext,ov}} \) as illustrated in Fig. 2. As the channel dopant concentration \(N_A\) increases, \( C_{\text{df}} \) decreases and \( L_{\text{ext,ov}} \) will approach \( L_D \). The total channel length loss \( \Delta L = \Delta L_{\text{AEI}} + 2L_{\text{ext,ov}} \) is also illustrated to show the poly gate etch variation among devices. \( \Delta L_{\text{AEI}} \) is the poly gate etch loss.

B. Determination of the Drain-and-Source Series Resistance

An MOS device can be considered as an intrinsic MOS device in series with two resistors \( R_S \) and \( R_D \) as shown in Fig. 3 where \( R_S \) and \( R_D \) are the series resistances at source and drain terminals, respectively. Based on the I-V equation in the linear region

\[
I_D = W C_{OX}(V_{GS} - V_T - 0.5V_{PD}) \times \frac{\mu_{\text{eff}}(V'_G, V'_D, N_{\text{SUB}}) V'_D}{L_{\text{eff}}} (9)
\]

where \( L_{\text{eff}} \) is \( L_{\text{int,ch}} \) as derived by (1). The effective mobility of the inversion carriers \( \mu_{\text{eff}} \) is bias-dependent \((V'_G, V'_D)\) and substrate-doping-dependent \((N_{\text{SUB}})\). \( V'_G \) is the gate over-
From (18), \( V'_{GS} \) and \( V'_{DS} \) in the inversion carrier density, \( C_{OX}(V'_{GS} - V_T - 0.5V_{DS}) \) and effective mobility, \( \mu_{eff} \), can be replaced by \( V_{DS} \) and \( V_{GS} \). Hence, the measured drain current \( I_D \) in (9) can be formulated by

\[
I_D = W C_{OX}(V_{GS} - V_T - 0.5V_{DS}) \times \mu_{eff}(V_{GT}, V_{DS}, N_{SUB})V_{DS}/L_{eff}.
\]

(19)

For an ideal case with zero \( R_S \) and \( R_D \), the external drain internal biases \( V_{DS} \), \( V_{GS} \) and the external biases \( V_{DS} \), \( V_{GS} \) are consumed across the extrinsic overlap region given by

\[
V'_{DS} = V_{DS} - I_D(R_D + R_S)
\]

(10)

and

\[
V'_{GS} = V_{GS} - I_D R_S
\]

(11)

where

\[
R_S = R_{sh}(V_{GT}) + R_C
\]

(12)

\[
R_D = R_{sh}(V_{GT}, V_{DS}) + R_C
\]

(13)

\[
R_{sh}(V_{GT}) = (R_{sh} + R_{sp})s
\]

(14)

\[
R_{sh}(V_{GT}, V_{DS}) = (R_{sh} + R_{sp})d
\]

(15)

and

\[
R_{DS} = R_D + R_S = R_d + R_S + 2R_C.
\]

(16)

Here, \( R_{sh} \) and \( R_{sp} \) are sheet resistance and spreading resistance as depicted in Fig. 3. These two resistances account for the bias dependence of \( R_{DS} \).

For the device operating in the linear region, \( V_{DS} \ll V_{GS} - V_T \), i.e., the depletion due to \( V_{DS} \) is negligible, then the series resistances can be considered nearly the same at the source and drain, i.e.,

\[
R_{DS} = 2R_s + 2R_C = 2R_S
\]

(17)

and then, from (10), (11), (16), and (17)

\[
V'_{GS} - V_T - 0.5V'_{DS} = V_{GS} - V_T - 0.5V_{DS}.
\]

(18)

\[\text{Fig. 2. The extrinsic overlap length } 2L_{ext,ov} \text{ and total channel length loss } \Delta L = \Delta L_{AL} + 2L_{ext,ov} \text{ extracted by decoupled C-V method.} \]

\[\text{Fig. 3. The device cross section and equivalent circuit of an intrinsic MOSFET in series with the drain and source series resistance, } R_D \text{ and } R_s.\]

\[\text{In this section, we will show the characterization results of the effective channel length and bias-dependent D/S series resistance achieved by the new approach. The extended application in the I-V model will also be demonstrated. Comparison between the measured and modeled I-V characteristics has been made for both SD and LDD devices.}\]
centtion within $L_{ext,ov}$ is higher than $N_A$ while that within $L_{int,cl}$ is below $N_A$. Therefore, in the I-V characteristics, $V_{int,ov}$ keeps below the DC threshold voltage, $V_T$, to avoid the turn-on of DC conduction and minimize the gate modulation effect on the extrinsic overlap region. That is not possible to be achieved by the conventional I-V method. The inherent advantage of this decoupling scheme is that the earlier inversion region is separated as the extrinsic overlap region so that the modeling for the intrinsic channel region can be simplified. As listed in Table I, $L_{ext,ov}$ and $L_{int,cl}$ have been determined for 0.7 $\mu$m SD MOSFET’s with splittted channel implant doses. Obviously, $L_{ext,ov}$ shrinks and then $L_{int,cl}$ increases with increasing $N_A$. As $N_A$ increases to a very high value, $L_{int,cl}$ will approach $L_j$ due to the fact that 2D charge sharing effect is greatly relieved and $L_{ext,ov}$ approaches the value of $L_D$. Furthermore, this method is also verified on scaled LDD devices. A successful application based on $L_{eff} = L_{int,cl}$ will be demonstrated by the accurate I-V characterization for submicron devices in Section IV-C.

The ideal $I_D - V_{GS}$ are calculated based on $L_{eff} = L_{int,cl}$ and bias-dependent effective mobility, $\mu_{eff}(V_{GT}, N_{SUB})$, extracted from the $I_D - V_{GS}$ characteristics of long channel devices under low drain operation ($V_{DS} \ll V_T$). This approach has been justified in the previous paper [14] by that the C-V characteristics of the intrinsic channel region can be well modeled by the ideal quasi-static C-V theory. It guarantees that the earlier inversion induced by 2D charge sharing effect is excluded completely from the intrinsic channel region. Therefore, the low drain mobility extracted from long channel devices can be used for the intrinsic channel region with the length, $L_{int,cl}$, scaled down to submicron regime, if the channel implant dose keeps low enough to avoid reverse short channel effect [15]. According to this decoupling algorithm, the 2D charge sharing effect in the extrinsic overlap region with a length of $2L_{ext,ov}$ is represented by the bias-dependent $R_{DS}$ in the I-V model.

B. Bias-Dependent Drain-and-Source Series Resistance

Fig. 4 makes a comparison between the ideal $I_D - V_{GS}$ and the measured $I_D - V_{GS}$ for SD MOSFET ($L_M = 0.7 \sim 1.2 \mu$m, $N_A = 5.2 \times 10^{15}$ cm$^{-3}$). A pronounced current drive degradation from $I_{D0}$ to $I_D$ is ascribed to the bias consumption across the series resistance $R_{DS}$. From (21b), $R_{DS}$ can be determined. Fig. 5(a) shows obviously that $R_{DS}$ extracted individually for each device is channel-length-independent. Fig. 5(b) demonstrates $R_{DS} = V_{GT}$ characteristics for SD devices with $N_A = 5.2 \times 10^{15} \sim 1.0 \times 10^{17}$ cm$^{-3}$. Gate bias dependence and channel-doping dependence are observed and the bias dependence is channel-doping dependent. For the most lightly doped case ($N_A = 5.2 \times 10^{15}$ cm$^{-3}$), the most serious gate bias dependence is observed. The maximum $R_{DS}$ at small $V_{GT}$ reaches about $4 \times 10^3$ $\Omega \mu$m and decays to about $1.5 \times 10^3$ $\Omega \mu$m with gate bias increased to $V$. As the channel doping is increased to a higher value ($N_A = 1 \times 10^{17}$ cm$^{-3}$), the bias dependence is greatly alleviated. The maximum $R_{DS}$ at small $V_{GT}$ is sensitive to $N_A$ and can be effectively reduced with increasing $N_A$. The decrease of maximum $R_{DS}$ with increasing $N_A$ is consistent with the shrinkage of $L_{ext,ov}$ as shown in Table I and Fig. 2. The decay of $R_{DS}$ with increasing gate bias is attributed to the enhanced conductivity modulation across the extrinsic overlap region (the source/drain lateral diffusion region and earlier inversion region). This decay of $R_{DS}$ saturates with the gate bias increasing continuously, and a residual resistance is observed to be weakly dependent on channel doping concentration. As for LDD NMOS device, a typical $R_{DS} = V_{GT}$ characteristics is demonstrated in Fig. 6. The bias dependence is much more serious than that of SD devices. The maximum $R_{DS}$ reaches a very high value of about $8 \times 10^5$ $\Omega \mu$m, just doubles that of SD devices with the most lightly doped channel ($N_A = 5.2 \times 10^{15}$ cm$^{-3}$). This pronounced bias dependence of $R_{DS}$ encountered in LDD devices is not easy to be modeled physically, since the lateral diffusion profile of the LDD region is in essence a 2D problem. In conclusion, $R_{DS} = V_{GT}$ ($N_{SUB}$) can be derived accurately from the measured $I_D - V_{GS}$ and calculated $I_{D0} - V_{GS}$ based on $L_{eff} = L_{int,cl}$, and bias-dependent effective mobility $\mu_{eff}(V_{GT}, N_{SUB})$.

C. The Analytical I-V Model for Submicron Devices

An analytical I-V model is formulated by (9) covering from linear to saturation region, in which $L_{eff}$, $R_{DS}$, and $\mu_{eff}$ are three key parameters to be determined and modeled. The impact of $L_{eff}$ and $R_{DS}$ on the I-V characteristics increases with the channel length scaling down. Therefore, the accuracy of I-V model for submicron devices depends critically on the accurate determination of $L_{eff}$ and $R_{DS}$, and modeling for the bias-dependent $R_{DS}$. An empirical model, $R_{DS} = R_0 + \alpha V_{GT}^{-\beta}$, is proposed for the bias-dependent $R_{DS}$ of SD and LDD MOSFET based on the experimental results obtained by the decoupled C-V method as demonstrated in Fig. 5 and Fig. 6. $R_0$ is a residual resistance at very high $V_{GT}$. It is observed to be bias-independent and weakly dependent on channel doping concentration. $\alpha$ and $\beta$ are channel doping dependence parameters. As high drain operation is concerned, $R_{DS}$ model has been modified to be $R_D = 0.5[R_0 + \alpha (V_{GT} - V_{DS})^{-\beta}]$ and $R_S$ keeps the linear region formula, $0.5[R_0 + \alpha (V_{GT} - V_{DS})^{-\beta}]$. Carrier depletion due to increasing $V_{DS}$ is considered in the inversion
carrier density, \( Q_{inv} = C_{ox}(V_{GS} - V_T - 0.5V_D) \). This bias-dependent \( Q_{inv} \) and velocity saturation effect have been implemented in a physically based mobility model \([16]-[17]\) by analytical formulas to account for high drain operation. Figs. 7(a) and (b) demonstrate that the analytical model can predict the I-V characteristics in linear region for the submicron devices \((L_M = 0.7 \, \mu m)\) with both SD and LDD structures and with wide range of channel dopant concentrations \((5.2 \times 10^{15} - 1 \times 10^{17} \, cm^{-3})\) accurately. This \( R_{DS} \) model extendible to high drain region is also verified on the \( I_D - V_{DS} \) characteristics. Fig. 8 shows a good match is achieved between the model and the experimental. To exemplify the accuracy and advantage gained from this new approach, the modeled results using \( L_{eff} = L_{ij} \) and constant \( R_{DS} = R_0 \) are demonstrated in Fig. 9 for SD devices with various \( N_A \) in comparison with Fig. 7(a). Serious deviation from the experimental I-V is observed and the deviation is aggravated by decreasing \( N_A \). It can be understood easily from the \( N_A \) effect on the relationship between \( L_{ij} \) and \( L_{int, ch} \) (discussed in IV-A) and \( N_A \) effect on \( R_{DS} - V_{GT} \) characteristics demonstrated in Fig. 5. As \( N_A \) decreases, 2D charge sharing effect is aggravated so that \( L_{int, ch} \) shrinks (due to the increase of \( L_{ox, ch} \)) and is much smaller than \( L_{ij} \). As a consequence, the use of \( L_{eff} = L_{ij} \) becomes inadequate. As for the \( R_{DS} \) model, the bias dependence of \( R_{DS} \) is also aggravated with decreasing \( N_A \), thus constant \( R_{DS} \) is not adequate in this case and will result in serious deviation from the experimental I-V characteristics.
D. The Advantages of the New Approach
Over the Conventional I-V Method

The major advantages of the decoupled C-V method over the conventional I-V method are three-fold. First, $I_{\text{short-circ}}$ (or $\Delta L$) extracted by the decoupled C-V method is with the gate biased under subthreshold condition, i.e., $|V_{\text{GS}}| = |V_{\text{int, on}}| < |V_{\text{T}}|$ and with $V_{\text{DS}} = 0$ (source/drain are tied together) to keep zero DC current. Therefore, in the determination of $L_{\text{eff}}$, voltage drop across $R_{\text{DS}}$ is avoided and then $R_{\text{DS}}$ variation induced error is eliminated. Secondly, the demand for precise $V_T$ extraction and the associated difficulty is alleviated although it is crucial for the accuracy of I-V method to keep a small and constant gate overdrive $V_{\text{GT}}$. For I-V method, constant $V_{\text{GT}}$ is required to keep the same channel resistivity (inversion carrier density and effective mobility $\mu_{\text{eff}}$), however, the extraction of $V_T$ and $\mu_{\text{eff}}$ is generally complicated by the short channel effects and generates another error source. The controversies as described are inherently existing in the I-V method and motivate many investigations on this topic [1]-[13]. As for the decoupled C-V method, the basic parameters such as $L_{\text{eff}}$ and $N_T$ can be determined accurately [14], [15] due to $R_{\text{DS}}$ effect is excluded and $V_T$ can be calculated from $N_T$ (or $N_D$) precisely. Thirdly, bias-dependent mobility model for this effective channel region can be greatly simplified, since the carrier transport in the early inversion region with higher $V_{\text{GT}}$ is modeled by the bias-dependent behavior of $R_{\text{DS}}$ separately. In contrast, for the conventional I-V method, mobility model is complicated by lumping $R_{\text{DS}}$ effect into itself and the unjustified approximation for $R_{\text{DS}}$ does not account for the 2D effect successfully.

VI. CONCLUSION

The effective channel length and bias-dependent drain-and-source series resistance have been successfully determined by the new C-V approach. For the first time, the difficulties encountered in the conventional I-V method can be solved effectively. It is attributed to that no DC current is required for the extraction of the effective channel length and then the error originated from the assumption of a constant D/S series resistance can be eliminated completely. The 2D charge sharing effect is incorporated into the bias-dependent $R_{\text{DS}}$. This bias dependence is closely related to the drain/source doping profile and the channel dopant concentration. A semi-empirical model can be derived from the bias-dependence of D/S series resistance and gives an accurate description for the two dimensional effect.

An analytical I-V model has also been developed based on the effective channel length, bias-dependent D/S series resistance and a physically based mobility model. Excellent agreement with the experimental I-V has been extensively verified on the submicron MOS devices with both SD and LDD structures and with wide range of channel doping concentrations. The characterization of $L_{\text{eff}}$ and $R_{\text{DS}}$ achieved by this new approach keeps both accuracy and simplicity to be well suited for circuit simulation and device design.

REFERENCES


Fig. 8. Comparison of $I_D - V_{GS}$ characteristics between measured and analytical model results for 0.7 um NMOS ($L_{\text{on}} = 0.66$ um, $L_{\text{eff}} = 0.39$ um, and $N_T = 5.3 \times 10^{16}$ cm$^{-2}$).

Fig. 9. Measured $I_D - V_{GS}$ characteristics using $L_{\text{off}} = L_{\text{on}}$ and constant $R_{\text{DS}}(= R_{\text{t}})$ and the comparison with measured results for 0.7 um SD NMOS, $L_{\text{eff}}(N_T = 5.2 \times 10^{11}) = 0.53$ um, $L_{\text{eff}}(N_T = 5.3 \times 10^{11}) = 0.54$ um, $L_{\text{eff}}(N_T = 1.0 \times 10^{11}) = 0.36$ um.
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