A Fault-Tolerant PMSG Drive for Wind Turbine Applications With Minimal Increase of the Hardware Requirements

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Abstract—Fault-tolerant permanent magnet synchronous generator (PMSG) drives for wind turbine applications play a major role in improving reliability and availability levels, since power converters are very prone to fail. In this paper, a fault-tolerant converter with the ability to handle power switch open-circuit faults is addressed. The main concern of the proposed converter topology is the minimization of the hardware requirements, leading to a low increase of the system cost. First, the employed fault diagnostic technique does not require additional measurements, nor high computational effort. Secondly, the circuit topology reconfiguration implies a minimum number of extra components as well as minimal oversizing of the standard ones. Accordingly, a four-switch three-phase converter with the dc bus midpoint connected to the transformer neutral point and a three-switch three-phase rectifier are adopted for post-fault operation of the grid- and PMSG-side converters, respectively. Vector control strategies are proposed for both converters under analysis, focusing the issues of capacitor voltages balancing and torque ripple minimization. The performance of the proposed fault-tolerant PMSG drive is analyzed by means of experimental results.

Index Terms—Fault-tolerant systems, permanent-magnet machines, wind power generation.

I. INTRODUCTION

PERMANENT-MAGNET synchronous generator (PMSG) drives have achieved prominence in wind energy conversion systems for offshore application, where increased reliability and availability are mandatory. However, the employed power converters have contributed to failure rates of modern wind turbines higher than expected [1]. A majority (≈ 60%) of those failures is associated with semiconductor or control circuit faults [2]; and the industry demands a solution to such issues [3]. Thus, cost-effective fault-tolerant systems with the ability to handle unforeseen open-circuit faults are needed, allowing the reduction of the wind energy cost by preventing unplanned stoppages and increasing the availability.

A fault-tolerant converter is intended to maintain its operation after an internal fault until a maintenance operation can be scheduled, with an acceptable performance and without endangering the overall system. Generally, both hardware and software need to be reconfigured for an effective post-fault control of the power converter. Various topologies have been proposed to endow a standard three-phase converter with fault-tolerant capabilities, by including a redundant leg connected to all the converter phases through TRIACs [4], [5] or to the machine neutral point [6], and by connecting the midpoint of the dc bus to the converter phases [7], [8] or to the machine neutral point [9]. Furthermore, in a back-to-back converter, the connection of the phases of both sides (grid/machine) to each other through TRIACs [10] has been also proposed. All these topologies have extra hardware requirements, additional components as well as the oversizing of the standard ones. Regarding their economic viability, the minimization of the extra hardware requirements assumes a paramount importance, which was elected as the selection criterion of the fault-tolerant converter topology proposed in this paper.

To eliminate the need for additional hardware, a three-switch three-phase rectifier (TSTPR) is adopted for post-fault operation of the generator-side converter. Such topology was proposed in [11], [12] as a grid-connected rectifier, and in [13], [14] for low-cost PMSG drives, but the generator torque ripple and its minimization have not been analyzed. Concerning the grid-side converter, the increase of hardware requirements is minimized through a four-switch three-phase converter (FSTPC) with the dc bus midpoint connected to the grid-side transformer neutral point. Although this topology has already been proposed for motor control [9], its output voltage limitation in comparison with the conventional six-switch voltage source has not been addressed comprehensively, which is essential to define the dc bus voltage increase of a grid-connected converter. In comparison to the fault-tolerant PMSG drive proposed in [15], the topology proposed in this paper for post-fault operation of the grid-side converter has a higher voltage capability, requiring a lower increase of the dc-link voltage as well as fewer extra components. Concerning post-fault operation of the PMSG-side converter, the same converter topology is chosen, but a simpler vector control strategy is proposed in this paper.
The aims of this paper are: (1) to investigate the requirements and limitations of the proposed topology; (2) to propose improved vector control techniques, taking into account the issues of capacitor voltages balancing and torque ripple minimization; and (3) to evaluate the performance of the proposed techniques.

II. FAULT-TOLENT CONVERTER TOPOLOGY

The fault-tolerant converter is composed of two six-switch three-phase converters (SSTPCs) in a back-to-back topology, each one comprising six IGBTs with the respective antiparallel diodes, and one additional TRIAC (Fig. 1(a)), which remains open under normal operating conditions. The included TRIAC is intended to reconfigure the circuit topology of the grid-side converter, which is a mandatory action after the occurrence of an open-circuit fault at an inverter stage, because there is no path through the affected phase for the current flowing in both directions. On the other hand, given a similar scenario in the generator-side converter, an alternative path for the current is available through the diodes, hence, additional hardware is avoidable. Therefore, an FSTPC and a TSTPR are suggested for the post-fault operation, for instance, if open-circuit faults occur on both converter sides in the upper IGBT of phases $A$ and $a$, the post-fault topology is shown in Fig. 1(b).

A reliable and effective fault diagnosis performed in real-time (without requiring additional hardware, nor a great increase in the computational burden) is crucial in a fault-tolerant system to trigger the remedial procedures. Accordingly, the diagnostic methods proposed in [16] are adopted in this paper, to identify the faulty phase in the grid-side and to localize the faulty switch in the PMSG-side.

III. FAULT-TOLENT GRID-SIDE CONVERTER

The detection of the faulty phase is followed by its isolation (inhibition of its control signals). Then, the connection of the transformer neutral point to the dc bus midpoint through the TRIAC (hardware reconfiguration) takes place, and finally, the software reconfiguration, by imposing proper references for the dc bus voltage and the phase currents. The following analysis of the FSTPC intends to present its voltage and current limitations in comparison with the six-switch three-phase converter. Moreover, the reference currents calculation for the three possible case scenarios of post-fault operation are presented, and the issue of capacitor voltages balancing is addressed through the manipulation of the reference currents.

A. Four-Switch Three-Phase Converter With the DC-Link Midpoint Connected to the Transformer Neutral Point

Analyzing the FSTPC in Fig. 1(b) (grid-side converter), it can be inferred that both capacitors of the dc link must assume a voltage value higher than the peak phase-to-neutral voltage ($V_{ph-n}$) at the converter output (transformer windings connected in wye), allowing the current control. Thus, the dc bus voltage for the FSTPC ($V_{dc}$) should be higher than $2V_{ph-n}$, which, compared with the standard six-switch three-phase converter (where $V_{dc} > \sqrt{3}V_{ph-n}$), results in an increase of approximately 15% [17]: $V_{dc}/V_{dc} = 2/\sqrt{3} \approx 1.15$.

On the other hand, the usable maximum output voltage can be analytically deduced through the voltage space vectors synthesized by the converter

$$V_c = \frac{2}{3}(u_{AN} + u_{BN}e^{j2\pi/3} + u_{CN}e^{j4\pi/3}) = u_{ca} + ju_{c\beta} \quad (1)$$

where $u_{AN}$, $u_{BN}$, and $u_{CN}$ stand for the phase-to-neutral voltages, which for the case where phase $A$ is isolated ($i_A = 0$) can be expressed by

$$u_{AN} = V_{ph-n}\sin(\omega t)$$
$$u_{BN} = V_{dc}\left(S_B - \frac{1}{2}\right)$$
$$u_{CN} = V_{dc}\left(S_C - \frac{1}{2}\right) \quad (2)$$
where \( V_{dc} \) is the dc bus voltage and \( S_A, S_B \) and \( S_C \) are the switching states (ON: 1, OFF: 0) of the upper IGBTs (\( I_1, I_3, I_5 \)) of phases \( A, B, \) and \( C \), respectively, with the switching states of the bottom switches (\( I_2, I_4, I_6 \)) being complementary to \( S_A, S_B \) and \( S_C \). Therefore, by substituting (2) in (1), the following voltage vectors in \( \alpha \beta \) axes can be deduced:

\[
\begin{align*}
 u_{c\alpha} &= \frac{V_{dc}}{3}(1 - S_B - S_C) + \frac{2}{3}V_{ph-n}\sin(\omega t) \\
 u_{c\beta} &= \frac{V_{dc}}{\sqrt{3}}(S_B - S_C)
\end{align*}
\]

and presented in Table I for the available switching states. Since the voltage space vectors do not only depend on the converter switching states [Fig. 2(b)], to guarantee that \( u_{1\alpha} \) (\( \alpha \)-axis component of \( V_1 \)) always assumes positive values as well as \( u_{1\beta} \) (\( \alpha \)-axis component of \( V_3 \)) assumes negative values, the following relationship must be verified:

\[
V_{dc}^r > 2V_{ph-n}
\]

where \( V_{dc}^r \) stands for the post-fault dc-link voltage. Therefore, to achieve the same maximum voltage than for an SSTPC, as a consequence of the fundamental current flow through the capacitors, which leads \( u_{dc1} \) and \( u_{dc2} \) (voltages of capacitors \( C_1 \) and \( C_2 \) [Fig. 1(a)], respectively) to be different from \( V_{dc}/2 \). Accordingly, by considering that \( V_{dc} = u_{dc1} + u_{dc2} \) assumes a constant value, the deviation of each capacitor voltage is defined as

\[
\Delta u_{dc} = \frac{u_{dc1} - u_{dc2}}{2}
\]

and, consequently, the capacitor voltages are given by

\[
\begin{align*}
 u_{dc1} &= \frac{V_{dc}}{2} + \Delta u_{dc} \\
 u_{dc2} &= \frac{V_{dc}}{2} - \Delta u_{dc}
\end{align*}
\]

Then, by expressing \( u_{BN} \) and \( u_{CN} \) as functions of \( u_{dc1} \) and \( u_{dc2} \)

\[
\begin{align*}
 u_{BN} &= u_{dc1}S_B + u_{dc2}(S_B - 1) \\
 u_{CN} &= u_{dc1}S_C + u_{dc2}(S_C - 1)
\end{align*}
\]

the space voltage vectors can be recalculated by using (1), allowing to verify that \( u_{c\beta} \) remains unchanged [as given by (3)], whereas \( u_{c\alpha} \) is given by

\[
u_{c\alpha} = \frac{V_{dc}}{3}(1 - S_B - S_C) - \frac{2}{3}V_{ph-n}\sin(\omega t).
\]

Consequently, Table II is obtained and the following relationship must be verified:

\[
V_{dc}^\prime - \Delta u_{dc,max} > 2V_{ph-n}
\]

where \( V_{dc}^\prime \) stands for the post-fault dc-link voltage when considering a non-ideal dc bus, and \( \Delta u_{dc,max} \) stands for the maximum absolute value of \( \Delta u_{dc} \) over a fundamental period of the grid currents. Thus, the minimum dc-link voltage that ensures the converter controllability is given by \( V_{dc}^r = 2V_{ph-n} + \Delta u_{dc,max} \), and the resulting increase of \( V_{dc} \) by \( V_{dc}^\prime/V_{dc} = 2/\sqrt{3} + \Delta u_{dc,max}/(\sqrt{3}V_{ph-n}) \).

Fig. 2 is presented as an example, where the dc link is 15% increased for post-fault operation. It can be noticed that \( V_{dc} = 200 \) V would be the minimum dc-link voltage to satisfy (4) and to ensure post-fault operation, but \( V_{dc} \) has to be higher as a consequence of both the voltage drop in the output filter and the capacitor voltage oscillation (9). Therefore, by considering the need for approximately extra 10 V in the dc-link voltage for compensating the voltage drop and \( \Delta u_{dc,max} \) of 20 V, the same maximum output voltage is obtained under both normal and post fault operation if \( V_{dc} \) is increased to 230 V under post-fault operation, and, consequently, the inner circles of Fig. 2(a) and (b) have equal radius (\( r = r' \)). Thus, in comparison with the minimum dc-link voltage required for normal operation (\( \approx 183 \) V), an increase of approximately 25% of \( V_{dc} \) is mandatory. Finally, it is worth pointing out that this increase depends on the dc-link capacitor bank design, namely, its rated capacitance (Section V).

### B. Voltage-Oriented Control

Fig. 3 depicts the proposed voltage-oriented control (VOC) strategy with hysteresis current control. Regarding the current control under post-fault operation, the imposed reference currents are intended to generate a magnetomotive force equal to that obtained under normal operation (with a balanced three-phase sinusoidal current system). Therefore, the produced magnetic flux as well as the induced electromotive force can remain

**Table I**

<table>
<thead>
<tr>
<th>( u_{c\alpha} )</th>
<th>( u_{c\beta} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{dc}/3 + V_{ph-a}\sin(\omega t) )</td>
<td>0</td>
</tr>
<tr>
<td>( 2V_{ph-a}\sin(\omega t) )</td>
<td>( V_{dc}/\sqrt{3} )</td>
</tr>
<tr>
<td>( -1/3V_{ph-a}\sin(\omega t) )</td>
<td>0</td>
</tr>
<tr>
<td>( 2V_{ph-a}\sin(\omega t) )</td>
<td>( V_{dc}/\sqrt{3} )</td>
</tr>
</tbody>
</table>

**Table II**

<table>
<thead>
<tr>
<th>( u_{c\alpha} )</th>
<th>( u_{c\beta} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{dc} - 2\Delta u_{dc} )</td>
<td>0</td>
</tr>
<tr>
<td>( 2V_{ph-a}\sin(\omega t) )</td>
<td>( V_{dc}/\sqrt{3} )</td>
</tr>
<tr>
<td>( -V_{dc} + 2\Delta u_{dc} - 2V_{ph-a}\sin(\omega t) )</td>
<td>0</td>
</tr>
<tr>
<td>( 2V_{ph-a}\sin(\omega t) )</td>
<td>( V_{dc}/\sqrt{3} )</td>
</tr>
</tbody>
</table>
unchanged. Taking as an example a fault occurrence in phase \(A\), the phase \(A\) current becomes null after the fault isolation, and the same current space vector \((i_g = i_B e^{2j\pi/3} + i_C e^{j4\pi/3})\) is achieved if

\[
\begin{align*}
    i_B &= \sqrt{3}I_m \cos \left( \omega t + \phi - \frac{2\pi}{3} - \frac{\pi}{6} \right) \\
    i_C &= \sqrt{3}I_m \cos \left( \omega t + \phi + \frac{2\pi}{3} + \frac{\pi}{6} \right)
\end{align*}
\]

(10)

where \(I_m\) is the currents amplitude under normal operating conditions, \(\omega\) is the currents angular frequency and \(\phi\) is the initial phase angle. Thus, the phase currents increase by a factor of \(\sqrt{3}\), while the neutral current is three times higher: \(i_N = i_B + i_C = 3I_m \cos(\omega t + \phi + \pi)\). Therefore, to meet the grid connection requirements under post-fault operation, for the three distinct case scenarios of phases \(A\), \(B\), and \(C\) affected by an open-circuit fault, the reference phase currents \((i^*_A, i^*_B, i^*_C)\) are respectively given by

\[
\begin{align*}
    i^*_B &= \sqrt{3} \left[ -i^*_d \cos \left( \theta + \frac{\pi}{6} \right) + i^*_q \sin \left( \theta + \frac{\pi}{6} \right) \right] \\
    i^*_C &= \sqrt{3} \left[ -i^*_d \cos \left( \theta - \frac{\pi}{6} \right) + i^*_q \sin \left( \theta - \frac{\pi}{6} \right) \right] \\
    i^*_A &= \sqrt{3} \left[ i^*_q \cos \left( \theta + \frac{\pi}{6} \right) - i^*_d \sin \left( \theta + \frac{\pi}{6} \right) \right] \\
    i^*_B &= \sqrt{3} \left[ i^*_q \cos \left( \theta - \frac{\pi}{6} \right) - i^*_d \sin \left( \theta - \frac{\pi}{6} \right) \right] \\
    i^*_C &= \sqrt{3} \left[ -i^*_d \cos \theta - i^*_q \sin \theta \right] \\
    i^*_A &= \sqrt{3} \left[ i^*_q \cos \left( \theta - \frac{\pi}{6} \right) - i^*_d \sin \left( \theta - \frac{\pi}{6} \right) \right]
\end{align*}
\]

(11-13)

where \(\theta\) is the angular position of the grid voltage vector, and \(i^*_d\), \(i^*_q\) are the reference currents in the synchronous reference frame (outputs of the reactive power and dc-link voltage controllers, respectively).

C. Capacitor Voltage Balancing

Concerning the voltage oscillation, a proper design of the capacitor bank can provide an acceptable performance of the FSTPC, by limiting the maximum capacitor voltage oscillation. Nevertheless, the capacitor voltage deviation may force increased stress, due to an unbalanced current distribution through the two capacitors. Thus, the control of the capacitors voltage offset is crucial. This goal can be accomplished under hysteresis current control, by monitoring the voltage drift (through an additional voltage sensor) and by adding a dc offset \(i_0^*\) to the two reference currents \((i_j^*)\) given in (11)–(13), according to the error between the capacitor average voltages. Therefore, the switching states for each phase \(j\) are obtained as follows:

\[
S_j = \begin{cases} 
1, & i_j^* + i_0^* > i_j + BW_h/2 \\
0, & i_j^* + i_0^* < i_j - BW_h/2 
\end{cases}
\]

(14)

where \(BW_h\) stands for the hysteresis bandwidth. A positive value of \(i_0^*\) leads to the increased utilization of the switching state (11) and consequent discharge of the capacitor \(C_1\), whereas a negative value of \(i_0^*\) implies the increased utilization of the switching state (00), discharging \(C_2\). So, the center point voltage can be controlled by controlling the value of \(i_0^*\), which can be generated through an additional control loop with the average value of the error between the capacitor voltages as input of a proportional-integral controller (Fig. 3)

\[
\langle \Delta u_{dc} \rangle = f \int_0^\frac{1}{f} \left( \frac{u_{dc1} - u_{dc2}}{2} \right) dt = f \int_0^\frac{1}{f} \left( \frac{V_{dc} - u_{dc2}}{2} \right) dt
\]

(15)

where \(f\) stands for the grid fundamental frequency in hertz.

The neutral current flowing through the dc-link capacitors (for example, \(i_N = i^*_b + i^*_c + 2i_0^*\)) allows to control the capacitor voltage deviation according to

\[
\langle \frac{d}{dt} \Delta u_{dc} \rangle = -\langle i_N \rangle = \frac{-i_0}{C}
\]

(16)

where \(C\) stands for the capacitance of each dc-link capacitor \((C = C_1 = C_2)\).

The voltage control loop is depicted in Fig. 4, where the controller and dc-link transfer functions are given by

\[
C(s) = K_p + \frac{1}{T_i s}; \quad G(s) = \frac{1}{C s}
\]

(17)

To ensure stability of the closed-loop control system in Fig. 4, the PI controller parameters \((K_p, T_i)\) can be tuned by choosing a phase margin equal to 60°, for a given crossover.
frequency \( f_c \). The resultant controller parameters are then the following ones:

\[
T_i = \frac{2}{C(2\pi f_c)^2}, \quad K_p = \frac{\sqrt{3}}{T_i 2\pi f_c}.
\]

(18)

Regarding the choice of the crossover frequency, \( f_c \) should be lower than the grid frequency and also lower than the crossover frequency of the total dc-link voltage \((V_{dc})\) controller. This way the tuning of the two voltage controllers in Fig. 3 can be performed independently. The experimental results in Section VI were obtained with \( f_c = 2 \) Hz.

Additionally, to avoid the injection of a high dc component into the transformer phase currents, the controller output should be limited to low values. The amplitude of \( i_{0}^* \) is here limited to \( BW/2 \). It is worth noting that under steady-state the dc component present in the phase currents \((i_0)\) is null, due to the action of the PI controller. It should be pointed out that the proposed approach is similar to the one proposed for a Vienna rectifier in [18], [19]. However, the control of an FSTPC has no degree of freedom to control the center point voltage without adversely affecting its output currents.

### IV. Fault-Tolerant Generator-Side Converter

On the generator-side converter there is lack of need for hardware reconfiguration, and the fault isolation consists of the inhibition of the control signals of the three upper or bottom power switches, depending on whether an upper or a bottom IGBT is faulty, respectively. Although the fault isolation allows the generator to achieve a balanced operation (concerning the phase currents), the semi-controlled rectification leads to an increased distortion of the phase currents and oscillation of the generator electromagnetic torque. Therefore, to improve the performance of the rotor-field-oriented Control (RFOC) strategy for a TSTPR controlling a surface-mounted PMSG by reducing the torque oscillation, it is suggested to control \( i_{sd}^* \), instead of fixing it to zero to obtain the maximum torque per ampere.

#### A. Three-Switch Three-Phase Rectifier (TSTPR)

As discussed in [14], for a TSTPR controlling a PMSG, there are parts of the complex plane (Fig. 5) where a reduced number of converter voltage vectors are available, because the TSTPR works partially as a non-controlled rectifier. Consequently, the current control in one or two phases might be impossible, depending on the currents polarity, which implies that sinusoidal currents cannot be shaped. Taking as an example the case in which all upper IGBTs are in open-circuit [Fig. 1(b)], for the generator phase currents assuming positive values they must flow through the bottom diodes (freewheeling diodes \( R_2, R_4, \) and \( R_6)\). Thus, during the period of time in which a phase current is positive, the phase current flow is independent of the respective IGBT switching state as well as the phase-to-zero voltages

\[
u_{j0} = \begin{cases} V_{dc} S_j, & \text{if } i_j < 0 \\ 0, & \text{if } i_j > 0 \end{cases}
\]

(19)

First, it is not taken into consideration the case in which \( i_j = 0 \), and the phase voltages are expressed as follows:

\[
u_{an} = \frac{V_{dc}}{3} (2S_a n_a - S_b n_b - S_c n_c)
\]

\[
u_{bn} = \frac{V_{dc}}{3} (2S_b n_b - S_a n_a - S_c n_c)
\]

\[
u_{cn} = \frac{V_{dc}}{3} (2S_c n_c - S_a n_a - S_b n_b)
\]

(20)
where \( n_j \) defines if \( i_j \) is negative (\( n_j = 1 \)) or positive (\( n_j = 0 \))

\[
n_j = \frac{1 - \text{sgn}(i_j)}{2}
\]

and the sign function is given by

\[
\text{sgn}(i_j) = \begin{cases} 
1, & \text{if } i_j > 0 \\
-1, & \text{if } i_j < 0
\end{cases} \quad j = a, b, c.
\]

Lastly, the space voltage vectors in \( \alpha\beta \) axes are deduced as

\[
u_{ec\alpha} = \frac{V_{dc}}{3}(2S_a n_a - S_b n_b - S_c n_c)
\]
\[
u_{ec\beta} = \frac{V_{dc}}{\sqrt{3}}(S_b n_b - S_c n_c).
\]

It becomes clear that the converter space voltage vectors depend on the switching states as well as on the phase currents polarity. Since \( i_a + i_b + i_c = 0 \) implies that the three currents never assume negative values simultaneously, the available voltage vectors are limited to four, when two of the phase currents are negative, or to two, if only one is negative.

Moreover, if a phase current becomes null and the respective phase voltage is positive, it remains null till the phase voltage becomes negative and the bottom diode forward biased. During this time period the voltage in that phase is equal to the back electromotive force, and the converter generates a non-defined electromagnetic torque.

B. RFOC for a TSTPR With Torque Ripple Minimization

Through the mathematical model of a surface-mounted PMSG (SPMSG) in the synchronous reference frame, the stator voltage (\( u_s \)), the stator flux (\( \psi_s = \psi_{sd} + j \psi_{sq} \)), and the electromagnetic torque (\( T_e \)) are given by

\[
u_s = R_s i_s + j \omega_s \psi_s \approx j \omega_s \psi_s
\]
\[
\psi_{sd} = L_s i_{sd} + \psi_{PM} \\

\psi_{sq} = L_s i_{sq}
\]
\[
T_e = \frac{3}{2} p (\psi_{sd} i_{sq} - \psi_{sq} i_{sd}) = \frac{3}{2} p \psi_{PM} i_{sq}
\]

where \( i_{sd} \) and \( i_{sq} \) are the \( d \)- and \( q \)-axis stator currents (\( i_s = i_{sd} + j i_{sq} \)), \( L_s \) is the synchronous inductance (considering \( d \)- and \( q \)-axis inductances equal in a SPMSG), and \( \psi_{PM} \) is the permanent magnet flux. From now on, the stator resistance (\( R_s \)) is neglected (24), which is generally valid for high power machines as well as for low power machines operating in the high speed range.

Typically, in vector control strategies for SPMSGs, \( i_{sd} \) is set to zero to maximize the torque per ampere ratio [Fig. 6(a)]. Consequently, the displacement between \( i_s \) and \( \psi_s \) is load dependent, being reduced with the load increase (\( \delta \) increases). Thus, such control strategy applied to a TSTPR leads to a higher current distortion as the load increases (longer time periods with null current), consequently, the torque ripple also increases.

To achieve the minimum current distortion given by a constant displacement between \( i_s \) and \( \psi_s \) equal to 90° [Fig. 6(b)], the angle between the stator current space vector (\( i_s \)) and its \( q \)-axis component must be equal to angle between the stator and rotor flux space vectors (\( \delta' \)), verifying that

\[
\tan \delta' = \frac{|\psi_{sq}|}{|\psi_{sd}|} = \frac{|i_{sd}|}{|i_{sq}|} = \frac{|i_{sq}|}{L_s} - |i_{sd}|
\]

By solving the quadratic equation resulting from (27)

\[
-|i_{sd}|^2 + \frac{\psi_{PM}}{L_s} |i_{sd}| - |i_{sq}|^2 = 0
\]

to \( |i_{sd}| \), the absolute value of the \( d \)-axis stator currents is given as function of \( i_{sq} \) by

\[
|i_{sd}| = \frac{1}{2} \left[ \frac{\psi_{PM}}{L_s} - \sqrt{\left( \frac{\psi_{PM}}{L_s} \right)^2 - 4 |i_{sq}|^2} \right]
\]

with real solution for \( |i_{sq}| \leq \psi_{PM}/2L_s \). As a consequence of \( i_{sd} \) being different from zero, \( i_{sq} \) must be limited in accordance with

\[
i_{sq}^2 + \frac{I_s^2}{I_{sq}} \leq \frac{I_s^2}{I_{sq}}, \quad I_{sq} = \frac{2}{3} \frac{T_n}{p \psi_{PM}}
\]

to avoid exceeding the machine-rated current \( I_s \) (considered equivalent to the current generated at the rated torque \( T_n \) with \( i_{sd} = 0 \)). Then, by substituting (29) in (30), the new
maximum value of the stator current component responsible for the developed torque is obtained

\[ I'_{sq} = \frac{L_s}{\psi_{PM}} \sqrt{I_{sq}^2 \left( \frac{\psi_{PM}}{L_s} \right)^2 - I_{sq}^4}. \tag{31} \]

Accordingly, for an operation with \( i_{sd} \) equal to (29), a torque reduction factor can be defined by \( I'_{sq}/I_{sq} \).

With the aim to minimize the torque ripple, the \( d \)-axis stator current component can be generated in feedforward manner, by imposing the following reference value:

\[ i^*_{sd} = \frac{1}{2} \left[ \frac{\psi_{PM}}{L_s} - \sqrt{(\frac{\psi_{PM}}{L_s})^2 - 4i_{sq}^2} \right], \quad |i^*_{sq}| \leq I'_{sq} \tag{32} \]

where \( i^*_{sq} \) stands for reference \( q \)-axis current generated by the speed controller (Fig. 7). By using the reference value instead of the actual one of the \( q \)-axis current, an additional coordinate transformation is avoided as well as an additional low-pass filter to attenuate the noise presented in the measured currents. It should be pointed out that \( i^*_{sd} \) is always intended to be negative, for generator operation with positive speed and negative \( i_{sq} \) as well as with negative speed and positive \( i_{sq} \).

The block diagram of the proposed RFOC strategy with fault-tolerant capabilities is depicted in Fig. 7, where the fault diagnosis technique triggers the fault isolation and the control of \( i_{sd} \) by imposing (32) as reference value. The simple feedforward control of \( i_{sd} \) for reducing the torque ripple will work properly whether the error of the machine parameter estimation is negligible. In the case of a rough parameter estimation, it is recommended to select a higher value for \( \psi_{PM}/L_s \), avoiding an excessive increase of the stator current. It is worth noting that neglecting \( R_s \) in a low power machine operating at low speed has a similar contribution.

As an example, the machine parameters of Table IV are used to illustrate the impact of the proposed compensation method in the PMSG stator current \( |i_{sq}|(26), |i_{sd}|(29), \) and \( |i_s| \) are shown in Fig. 8 as function of the electromagnetic torque together with experimental results for three distinct load levels (25%, 50%, and 75% of the rated torque), using \( I_{sq} \) and \( T_n \) as base quantities. Fig. 8 shows that \( i_{sq} \) increases linearly with the torque, whereas \( i_{sd} \) increases quadratically. The rated current is achieved for a torque equivalent to 83% of \( T_n \), and at 89% of \( T_n \) the maximum real solution of \( |i_{sd}| \) is reached (which is fixed for higher torque levels, meaning that further compensation of the torque ripple is not performed).

### Table IV

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>2.2 kW</td>
</tr>
<tr>
<td>Speed</td>
<td>1750 rpm</td>
</tr>
<tr>
<td>Torque</td>
<td>12 Nm</td>
</tr>
<tr>
<td>Voltage</td>
<td>46 V</td>
</tr>
<tr>
<td>Current</td>
<td>10.4 A</td>
</tr>
<tr>
<td>Number of pole pairs</td>
<td>5</td>
</tr>
<tr>
<td>Armature resistance</td>
<td>0.415 Ω</td>
</tr>
<tr>
<td>Magnet flux linkage</td>
<td>0.121 Wb</td>
</tr>
<tr>
<td>Synchronous inductance</td>
<td>5.13 mH</td>
</tr>
</tbody>
</table>

V. Converter Design Considerations

Table V reveals the hardware requirements of the proposed fault-tolerant converter topology for PMSG drives together with three other topologies previously proposed in the literature that are suitable for PMSG drives, comparing them with the standard SSTPC. The criterion of choice used in Table V intends to minimize the hardware requirements increase, then, the system derating (if possible) is considered preferable for post-fault operation.

In the proposed topology, fault tolerance is achieved with a minimum of extra components (one TRIAC), and only with a significant increase of the dc-link capacitors current rating. To avoid oversizing the current ratings for the IGBTs and transformer, the maximum output power must be limited to 58% of the drive rated power \((1/\sqrt{3} \approx 0.58)\). Consequently, both TRIAC and neutral wire are sized for a current rating 73% higher than the converter phases. The required rated capacitance of each capacitor to limit the maximum voltage oscillation \((\Delta u_{dc,max})\) as a consequence of the low frequency current can be given by [9]

\[ C = \frac{\sqrt{3} I_{grid}}{2 \omega \Delta u_{dc,max}} \tag{33} \]

where \( I_{grid} \) stands for the rated current amplitude of the grid-side converter and \( \omega \) for the grid fundamental frequency. Finally, the capacitors maximum current can be obtained by following the design guidelines in [15] and taking into account that the low frequency current flowing through the capacitors is increased by a factor of \( \sqrt{3} \).

The requirement of a transformer in the proposed fault-tolerant drive can be seen as a disadvantage, because it may not be available and its inclusion would not be a cost-effective solution to achieve fault-tolerance. However, it is worth noting...
that the transformer is usually included at the converter output in high-power wind turbines with low-voltage two-level voltage source converters [20]. The transformer might be excluded if a medium-voltage multilevel converter is considered, which is still not the most common option nowadays.

Therefore, according to Table V, the fault-tolerant converter topology proposed in this paper is a cost-effective solution for wind turbine applications.

VI. EXPERIMENTAL RESULTS

The experimental setup is depicted in Fig. 9, which comprises a 2.2 kW PMSG (Table IV) coupled to a four-quadrant test bench, two Semikron SKiiP three-phase voltage source converters in a back-to-back topology, a 8 kVA three-phase core-type transformer, a TRIAC, a dSPACE DS1103 digital controller, two Yokogawa WT 3000 precision power analyzers, a dc bus capacitor bank of 1.1 mF \( (C = C_1 = C_2 = 2.2 \text{ mF}) \) and an output filter of 10 mH. Together with Matlab/Simulink and dSPACE ControlDesk software, the DS1103 controller provides real-time control and monitoring of the overall system with a sampling time of 50 s. An open-circuit fault is introduced by removing the IGBT gate command signal. The experiments were carried out at a grid phase-to-neutral voltage amplitude of 100 V (transformer-side with wye connection), a reference speed of 900 rpm and a load torque equivalent to 75% of the generator rated torque. A reference dc-link voltage of 200 V is imposed under normal operating conditions as well as under a fault in the PMSG-side converter, whereas it is increased to 230 V after a fault occurrence in the grid-side converter.

### A. Grid-Side Converter

Fig. 10 shows the system response to a fault in the IGBT \( I_1 \) of the grid-side converter at \( t = 0.11 \text{ s} \). Before the fault occurrence, the SSTPC topology provides a balanced three-phase current system as well as constant and balanced capacitor voltages. After the fault detection, which is performed in 1.75 ms (9% of the fundamental period), the remedial procedures are triggered, by turning off the phase A gate command signals, turning on the TRIAC, imposing new reference currents and increasing in 15% the reference dc-link voltage. As can be seen in Fig. 10 and Table VI, during post-fault operation the converter phase currents become \( \sqrt{3} \) times higher than during normal operation, while the neutral current is \( \sqrt{3} \) times higher than the phase current. The capacitor voltages \((u_{dc1}, u_{dc2})\) oscillates at the grid frequency (50 Hz), as a consequence of the current flow through the dc bus midpoint, but the average error between \( u_{dc1} \) and \( u_{dc2} \) is approximately null, thanks to the control of the capacitor voltages performed by introducing an offset in the reference currents (Section III-C). The reduction of the efficiency (converter, filter, and transformer) is attributed to both dc bus voltage and phase current increase. A practically unity power factor is always achieved.

### B. PMSG-Side Converter

Fig. 11 shows the electromagnetic torque behavior as a result of a fault occurrence, with an imposed delay time of 100 ms between each step of the fault-tolerant control for illustration purposes only. The fault (introduced at \( t = 0.16 \text{ s} \)) yields a pulsating electromagnetic torque, with a high pulsating component at the generator currents fundamental frequency. The fault isolation consists in removing the gate command signal of the upper IGBTs \((t = 0.26 \text{ s})\), resulting in the converter operation as a TSTPR. Despite balanced phase currents, they are highly distorted [Fig. 12(a) and (b)] and remain generating oscillating electromagnetic torque. Finally, the software compensation is considered, controlling \( i_{sd} \) with the aim to minimize both current distortion and torque ripple, which is effectively accomplished and well illustrated by Figs. 11 and 12.

The oscillation of the electromagnetic torque can be evaluated by the Total Waveform Oscillation: \( \text{TWO} = \)
TABLE VI
EVALUATION PARAMETERS OF THE GRID-SIDE CONVERTER

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Normal Operation Control</th>
<th>Fault-Tolerant Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMS Currents</td>
<td>Converter</td>
<td>3.05 A</td>
</tr>
<tr>
<td>Grid</td>
<td>1.58 A</td>
<td>1.72 A</td>
</tr>
<tr>
<td>Grid Power Factor</td>
<td>0.988</td>
<td>0.984</td>
</tr>
<tr>
<td>(V_{dc})</td>
<td>200 V</td>
<td>230 V</td>
</tr>
<tr>
<td>Efficiency</td>
<td>82.3 %</td>
<td>76.2 %</td>
</tr>
</tbody>
</table>

\[
\left(\frac{\sqrt{T_{e,\text{rms}}^2 - T_{e,\text{dc}}^2}}{|T_{e,\text{dc}}|}\right) \times 100\%
\]

where \(T_e\) is estimated with the knowledge of the stator flux and current by using (26), and \(T_{e,\text{rms}}\) and \(T_{e,\text{dc}}\) stand for the rms and average values, respectively. The torque TWO values for the considered operating conditions are presented in Table VII, confirming that the proposed control strategy permits a marked reduction of the torque ripple. The increase of the rms currents, when \(i_{sd}\) is different from zero, is also verified, which is reflected in a slight reduction of both generator and converter efficiencies.

VII. CONCLUSION

A cost-effective fault-tolerant PMSG drive has been proposed in this paper, since, by considering that an increase of 15% of the dc bus voltage is tolerated by the standard converter, the cost increase is only related to the additional TRIAC and the increase of the capacitors current rating.

Regarding the grid-side converter operation as a four-switch three-phase converter with the dc bus midpoint connected to the transformer neutral point, it was verified that considering an ideal dc link a voltage increase of 15% is required, but for a non-ideal dc link it may be higher. A vector control strategy...
with hysteresis current control and the ability to balance the capacitor voltages has been proposed.

For controlling a PMSG with a three-switch three-phase rectifier, a unity power factor based vector control strategy is proposed for torque ripple minimization, avoiding to exceed the generator rated current by limiting the maximum torque.

**TABLE VII**

<table>
<thead>
<tr>
<th>Evaluation Parameters of the PMSG-Side Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Operation</td>
</tr>
<tr>
<td>RMS Currents</td>
</tr>
<tr>
<td>PMSG Power Factor</td>
</tr>
<tr>
<td>Torque TWO</td>
</tr>
<tr>
<td>Efficiency</td>
</tr>
<tr>
<td>Converter</td>
</tr>
<tr>
<td>Generator</td>
</tr>
</tbody>
</table>

**Fig. 11.** Experimental results regarding the generator electromagnetic torque response to a fault in the PMSG-side converter with a delay time of 100 ms between each step of the fault-tolerant control, for illustration purposes only.

**Fig. 12.** Experimental results regarding the phase currents in the time-domain and in the stationary reference frame, during: (a) fault isolation and software compensation; (b) fault isolation ($i_{sd} = 0$); (c) software compensation (32).

**References**


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