A Capacitor-Charging Power Supply Using a Series-Resonant Topology, Constant On-Time/Variable Frequency Control, and Zero-Current Switching

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Abstract—Conventional dc power supplies are normally designed for constant power applications and do not perform well under the wide range of load variations involved in repetitively charging a capacitive load from zero volts to a maximum voltage. A power supply specifically designed for capacitor-charging applications that uses a series-resonant circuit topology, a constant on-time/variable frequency control scheme, and zero-current switching techniques has recently been developed. The performance of this capacitor-charging power supply (CCPS) has been evaluated in the laboratory by charging several values of load capacitance at various repetition rates. The CCPS has charged a 1-μF capacitor from 0–1500 Vdc in 750 μs, exhibiting a charging power of 1500 J/s. This operation has been repeated at a rate of 800 charges per second, which corresponds to an average power output of 900 W. A 10-μF capacitor has been charged from 0–1500 Vdc in 8 ms. These results indicate that this design is very feasible for use in capacitor-charging applications.

I. INTRODUCTION

ELECTRICAL equipment utilized in pulse power applications usually derives its bursts of energy by rapidly discharging a capacitor. Flashlamps, which may be used in sterilization or other applications that require flashes of high-intensity light, and pulsed lasers, which may be used in cutting or welding, both derive the required bursts of energy in this fashion. The capacitors used in these types of equipment are energy-storage capacitors and must be charged by a capacitor-charging power supply (CCPS) prior to each repetition of energy release to the load. Fig. 1 shows the voltage across the energy-storage capacitor connected to the output of the CCPS. As seen in this figure, the capacitor voltage is divided into two cycles; charge and discharge. During the discharge cycle, the CCPS is disabled while the capacitor is rapidly discharged by the load, which is inactive in the charge cycle. The discharge cycle is normally much shorter than the charge cycle. The CCPS enters the charge cycle with near short-circuit conditions across its output terminals and begins operation in the charging mode. In this mode, the CCPS operates at its maximum charging capability while charging the capacitor to the target voltage. The CCPS moves from the charging mode to the refresh mode when the target voltage is reached and remains in this mode until the load discharges the capacitor. The output voltage may drift due to capacitor leakage and parasitic resistances; the CCPS compensates for any drift by supplying a small current to the energy-storage capacitor. This current may be supplied continuously in a manner similar to trickle charging a battery or discontinuously in short bursts [1]–[3]. The refresh mode is important when the repetition rate, the frequency at which the load discharges the energy storage capacitor, is low.

In contrast to a conventional high-voltage dc power supply that delivers constant or near constant power to its load, the output power of the CCPS varies over a wide range [1], [2]. The charging mode is characterized by high peak power. The instantaneous output power is almost zero at the beginning of the charging mode, and, if the charging current is constant, the peak instantaneous output power occurs at the end of the charging mode. The refresh mode is typically a low-power mode because the currents are small compared to those in the charging mode. The average output power for a CCPS depends on the repetition rate and is a maximum when the capacitor is discharged at the end of the charging mode.

This paper describes a prototype capacitor-charging power supply that has been designed, assembled, and tested. First, a simplified diagram for the CCPS is presented and the theory of operation is discussed. Then, a more detailed circuit diagram is presented, and the practical implementation of each subcircuit is explained. Finally, experimental results

Fig. 1. Capacitor voltage.
obtained from the CCPS are presented, and the performance of the CCPS is evaluated for both single charge and repetitive charge cases.

II. THEORY OF OPERATION

Fig. 2 shows a simplified diagram of the power section of the CCPS. Shown in this figure are the series resonant inverter, consisting of \( S_1-S_2, \ D_1-D_4, \ L, \) and \( C; \) the high-voltage transformer; the output rectifier; the load capacitor \( C_l; \) and the pulsed load. The inverter section of the CCPS performs a dc-ac conversion of the input voltage so that the transformer can step the voltage up to the desired output level. The diode bridge rectifies the secondary current of the high-voltage transformer to provide the charging current for the load capacitor. The pulsed load discharges the load capacitor whenever it requires a burst of energy.

The inverter switches may be in one of three different configurations at any given time: 1) \( S_2 \) and \( S_3 \) may be closed (on) while \( S_1 \) and \( S_4 \) are open (off), 2) \( S_1 \) and \( S_4 \) may be on while \( S_2 \) and \( S_3 \) are off, or 3) all of the switches may be off. The antiparallel diodes (also known as freewheeling diodes) \( D_1-D_4 \) provide a path for the resonant current when the corresponding switches around which they are connected are off. During switching configuration 1), the inverter voltage \( V_{ab} \) is equal to \(+V_{BUS}, \) and the resonant current \( I_R \) flows through \( S_2 \) and \( S_4, \) in the positive direction. During switching configuration 2), \( V_{ab} = -V_{BUS,} \) and the resonant current is negative and flows through \( S_1 \) and \( S_3. \) During configuration 3), the value of \( V_{ab} \) depends on which pair of freewheeling diodes, if any, is conducting. If \( D_1 \) and \( D_3 \) are conducting, \( I_R \) is negative, and \( V_{ab} = +V_{BUS}. \) If \( D_1 \) and \( D_3 \) are conducting, \( I_R \) is positive and \( V_{ab} = -V_{BUS.} \) If \( I_R = 0 \) A, then none of the diodes is conducting.

The operation of the circuit in Fig. 2 may be divided into four modes based on which switches and diodes are conducting. An equivalent circuit is drawn for each mode assuming that all resistances are negligible, all switches and diodes are ideal, and the transformer is ideal. Mode 1 occurs when switches \( S_2 \) and \( S_4 \) are conducting and the resonant current \( I_R \) is positive. The equivalent circuit for this mode is given in Fig. 3(a). The load capacitor has been reflected through the high-voltage transformer to provide the charging current for the load capacitor at the beginning of the mode. In mode 2, which occurs when \( D_1 \) and \( D_3 \) conduct, the resonant current is negative. Fig. 3(b) shows the equivalent circuit for this mode. As the resonant current is now negative, the polarity of the voltage source \( u_1(t_0) \) is the opposite of mode 1 because of the operation of the output rectifier. Mode 3 is characterized by switches \( S_1 \) and \( S_3 \) conducting and a negative resonant current and is described by the equivalent circuit in Fig. 3(c). When diodes \( D_2 \) and \( D_4 \) conduct, the resonant current is positive and the circuit is operating in mode 4. Because the resonant current is positive, the polarity of the voltage source \( u_1(t_0) \) in Fig. 3(d) is the same as it is in (a).

In the steady-state analysis of series resonant converters supplying constant power loads, the transformer, output rectifier, and load are modeled as a constant voltage for all four modes. For a CCPS, however, the voltage \( u_1(t_0) \) changes very rapidly as the energy-storage capacitor is charged. Therefore, previous analyses that are based on the assumption of the constant voltage representation are not applicable in this case. The solution for the voltages and currents in any of the equivalent circuits in Fig. 3 may be obtained using standard circuit analysis techniques. For example, the current \( i_R(t) \) in mode 1 can be determined as follows [4]:

\[
i_R(t) = \frac{V_{BUS} - u_2(t_0) - u_3(t_0)}{Z_0} \sin \left[ \omega_0(t - t_0) \right] + i_R(t_0) \cos \left[ \omega_0(t - t_0) \right]; \quad t_0 < t \leq t_x \quad (1)
\]

where the characteristic impedance \( Z_0 \) and resonant frequency \( \omega_0 \) are given by (2), and \( t_0 \) and \( t_x \) are the start time and end time, respectively, for mode 1.

\[
Z_0 = \sqrt{\frac{L}{C_{eq}}} \quad \omega_0 = \frac{1}{\sqrt{LC_{eq}}} \quad (2)
\]

\( \omega_0 \) is the series combination of capacitors \( C \) and \( C_l. \) The reflected load capacitance \( C_l \) is equal to the product of the load capacitance \( C_l \) and the turns ratio of the transformer squared. As a result, in high-voltage applications \( C_l \) is much larger than the resonant capacitor \( C, \) thus \( C_{eq} \) is approximately equal to \( C \) for a wide range of load capacitances. This is an important reason for employing the series resonant converter in this application because it allows the CCPS to charge a wide range of load capacitances without affecting the characteristic impedance or resonant frequency of the converter. In comparison, if a parallel resonant converter [5] is utilized for capacitor charging, the reflected load capacitor is in parallel with the resonant capacitor. Therefore, the resonant frequency varies directly with the load capacitance connected to the output of the CCPS.

The voltage across the resonant capacitor and the reflected load capacitor for mode 1 can be found from [4]:

\[
u_2(t) = u_2(t_0) + \frac{1}{\omega_0 C} \left( \frac{V_{BUS} - u_2(t_0) - u_3(t_0)}{Z_0} \right)
\]

\[
\cdot \left[ 1 - \cos \left[ \omega_0(t - t_0) \right] \right] + i_R(t_0) \sin \left[ \omega_0(t - t_0) \right] \quad (3)
\]

\[
u_3(t) = u_3(t_0) + \frac{1}{\omega_0 C L} \left( \frac{V_{BUS} - u_2(t_0) - u_3(t_0)}{Z_0} \right)
\]

\[
\cdot \left[ 1 - \cos \left[ \omega_0(t - t_0) \right] \right] + i_R(t_0) \sin \left[ \omega_0(t - t_0) \right] \quad (4)
\]
The currents and voltages for the other modes are of the same form as those for mode 1. The only difference is the sign of some of the voltage terms. For instance, the sign of \( V_{i1} \) is positive for modes 1 and 2 and negative for modes 3 and 4. The sign of \( V_{i2}(t) \) is positive in modes 1 and 4 when the current is positive and negative in modes 2 and 3 when the current is negative.

In capacitor-charging applications, it is important to charge the load capacitor as rapidly as possible. The capacitor charge is directly related to the current flow through the resonant circuit and into the load capacitor. There exists a trade-off between the charging time for the capacitor and the rating of the components; the currents in the CCPS must be limited to a safe value while charging the capacitor rapidly. Examination of (1) shows that the characteristic impedance \( Z_0 \) may be utilized to limit the current. If \( Z_0 \) is selected large enough to limit the current at the beginning of the charge cycle when the output voltage is approximately zero, then the charge time is increased because the current will be reduced as the output voltage builds up to the target value. If, on the other hand, \( Z_0 \) is chosen so that the current is large enough to provide a large charging current as the output voltage approaches the target value, then the current at the beginning of the charge cycle may exceed the ratings of components in the CCPS.

Instead of selecting a value of \( Z_0 \), which is a compromise between limiting the current and providing a reasonable charging time, the switching frequency of the series-resonant converter may be varied with respect to the resonant frequency to control the current flow through the resonant circuit to the load capacitor [5]. The current flow through the resonant circuit is varied by changing the ratio of the switching frequency to the resonant frequency. This ratio may be held constant [2] or it may be varied [1], [3]. For a constant switching frequency, the ratio should be selected to limit the current at the beginning of the charge cycle and yet provide enough current to charge the capacitor quickly. The variable frequency scheme begins with a ratio that limits the current to a safe value at the beginning of the charge cycle. To increase current flow through the resonant circuit as the output voltage builds up, the switching frequency is moved toward the resonant frequency. The output voltage that increases as the capacitor is charged limits the current.

Examination of (1) indicates that the current for mode 1 is described by two sinusoidal components. If switches \( S_1 \) and \( S_2 \) are turned on for a sufficient time period, the current will reach zero and the devices will turn off at zero current, thus reducing switching losses. Zero-current switching is possible as long as the switching frequency is less than the resonant frequency. To ensure zero-current switching in the CCPS, the on-time of switches \( S_1 \) and \( S_2 \) and switches \( S_3 \) and \( S_4 \) is fixed to be equal to one-half of the resonant period \( T_0 \), which is the reciprocal of the resonant frequency. This on-time remains constant while the switching frequency is varied with respect to the resonant frequency to control current flow through the resonant converter.

The operation of the CCPS is shown in Fig. 4, which shows the output voltage of the CCPS \( (V_{\text{OUT}}) \), the signals that control the inverter switches (control signals A and B), the inverter voltage \( (V_{\text{IN}}) \), and the resonant current \( (I_R) \) for a complete charge cycle. When control signal A is high, the inverter is in configuration 1. When control signal B is high, the inverter is in configuration 2. When neither of these signals is high, the inverter is in configuration 3. As seen in the figure, the charge cycle is divided into two modes: charging and refresh, described as follows.

A. Charging Mode

The charging mode starts at the beginning of the charge cycle when the load capacitor is fully discharged and ends when the output voltage is equal to the target voltage. At the beginning of the charging mode, the CCPS operates into a near short-circuit load, as the output voltage is equal to zero volts. A slow start at the beginning of the charging mode limits the inrush current that results from the load capacitor...
being almost completely absent of charge. The slow start is implemented by gradually sweeping the switching frequency up to the maximum value, which is slightly less than the resonant frequency. The time constant of this slow-start function depends on the value of the load capacitor. Larger capacitors need longer slow-start times than smaller capacitors because more charge is required to build the output voltage up to a level that will limit the resonant current. When sufficient charge is accumulated on the load capacitor to limit the current to a value that is within the ratings of the switches, the inverter operates at the maximum switching frequency until the load capacitor voltage reaches about 90% of the target voltage \( V_T \). At this point, the switching frequency is gradually decreased proportionally to the increase in capacitor voltage until the target voltage is reached. Decreasing the switching frequency at the end of the charging mode decreases the chance of overshooting the target voltage at the beginning of the refresh mode. At the end of the charging mode when the output voltage has reached the target value, all inverter switches are turned off as the CCPS enters the refresh mode. As a result, one pair of switches may be required to turn off before the resonant current reaches zero. As the current is small at this instant because the output voltage is at the target value and the switching frequency has been reduced well below the resonant frequency, the switching losses at turn off are small.

Fig. 4 shows that regardless of the switching frequency, because the on-time of the switches is equal to one-half the resonant period, they always turn off when the current is equal to zero. Furthermore, certain frequencies allow zero current turn-on of the switches. During part of the slow-start time, the switching frequency may be low enough to allow a discontinuous current so the switches turn on at zero current. Also, when the switching frequency is at its maximum value, the current is nearly sinusoidal, and the switches turn on and off at zero crossings of the current.

**B. Refresh Mode**

Except for a small ripple voltage, the capacitor voltage is at the target value throughout the refresh mode until the load capacitor is discharged, at which time the CCPS reenters the charging mode after a brief delay. Charge is maintained on the capacitor during the refresh mode by minute packets of energy that compensate for losses due to parasitic resistances and capacitor leakage. Fig. 4 shows that during the refresh mode, the switching frequency is lower than it is for the charging mode and depends on the leakage rate of the load capacitor. Not indicated by Fig. 4, however, is that under certain circumstances, the on-time of the switches may be terminated prematurely (i.e., before the resonant current reaches zero). If the amount of energy required to refresh the load capacitor to the target voltage is less than that which can be delivered by the CCPS during half the resonant period, then the switches are turned off early to avoid overshooting the target voltage. This is the only instance in which zero current turn-off is not realized by the CCPS. Because the
refresh mode is a low-power mode, however, the current pulses are small in magnitude. Thus zero current switching is not as crucial during this mode as it is during the charging mode.

Equations (1), (3), and (4) describe operation of the converter in this mode also. The voltage $v(t_0)$ may now be treated as a constant in all equivalent circuits shown in Fig. 3. A simulation program [4] based on these equations has been utilized to study the performance of the converter in the refresh mode; this investigation indicates that the converter operates stably in that mode.

III. CIRCUIT DESCRIPTION

This section describes the prototype CCPS constructed and tested in the laboratory. The CCPS is designed for an output voltage of 1500 Vdc, a maximum switching frequency greater than 100 kHz, and an average output power of approximately 1 kW. This switching frequency allowed the leakage inductance of the transformer to be utilized as the resonant inductor $L$. The simulation program presented in [4] is used as an aid in the selection of the resonant capacitor $C$ and the slow start function in the charging mode.

Fig. 5 is a detailed circuit diagram of the CCPS consisting of the series-resonant inverter, the high-voltage transformer, the output rectifier, the feedback and control circuitry, the isolation stage, and the drivers for the inverter switches.

A. Series-Resonant Inverter

The inverter portion of the CCPS is made up of the four semiconductor switches $S_1$–$S_4$, their corresponding protection and snubber circuitry, a discrete capacitor, and the leakage inductance of the high-voltage transformer. The inputs of the inverter section are the dc input voltage $V_{BUS}$ and the drive signals for the switches. $V_{BUS}$ is derived by rectifying and filtering a 120-Vac line, which gives approximately a 160-Vdc input rail. The drive signals for the switches come from two half-bridge drivers that are discussed in Section III.B.

1) Switches: Each of the four switches consists of a parallel combination of two IRF250 HEXFET's, which have a voltage-blocking capability of 200 V and a current rating of 30 A. They contain an integral antiparallel Zener diode, which may serve both as a free-wheeling diode, carrying source-to-drain currents when the transistor is off and as protection against overvoltage. Parallel MOSFET's are used to increase the current ratings of the switches and, thus, the power rating of the CCPS. Although MOSFET's have significantly higher on-resistances than power bipolar transistors with comparable ratings, they were chosen for this design because of their fast switching times and their low-power drive requirements. All interconnections between the components of the bridge are made via a printed circuit board, which minimizes stray inductances.

The gate of each HEXFET is protected against overvoltage by two back-to-back Zener diodes, which limit the gate-to-source voltage of each transistor to $\pm 15$ V. The gate charging current is limited by a 10 $\Omega$ resistor $R_g$. This measure decreases the $dv/dt$ of the drain-to-gate voltage during switching. If the resistor $R_g$ was not present, then due to the large $dv/dt$ during transistor turn off, the drain-to-gate capacitance could force a large current spike out of the gate, which could damage the drive circuit and/or the transistor. The presence of $R_g$ also ensures that both HEXFET's in the parallel combination turn on and off during the same time interval. ($R_g$ is a 10-k$\Omega$ resistor connected between the gate and source of the switches to provide a bleed-off path for any stray charge that might accumulate on the gate-to-source capacitance of the MOSFET's while they are in the off state.

Series Schottky diodes $D_1$ and ultrafast recovery antiparallel diodes $D_2$ are included to prevent the relatively slow-body diodes of the HEXFET's from conducting. The long recovery times of the body diodes limit the operating frequency of the HEXFET's. The freewheeling effect is provided by $D_2$, whereas $D_1$ prevents the body diode from conducting. The antiparallel diodes need to have at least the same voltage and current ratings as the HEXFET's but the Schottky diodes are only required to block, at most, the forward voltage drop across the antiparallel diode. Thus $D_1$ may be a low-voltage diode with a current rating at least as great as that of the HEXFET's. Because both $D_1$ and $D_2$ have faster recovery times than the body diodes of the HEXFET's, higher operating frequencies are possible. The maximum switching frequency is not exactly equal to the resonant frequency because of the small amount of dead time that is required between switching configurations 1 and 2. This dead time is necessary to ensure that the semiconductors fully recover their blocking characteristics before the next set of switches is turned on [5]. Failure to provide a small amount of dead time could result in two series switches $S_1$ and $S_2$, for example, conducting simultaneously and short circuiting the input source. Such a situation would be catastrophic to the switches.

The snubber circuits consisting of $R_s$ and $C_s$ are included to reduce switching stresses in the semiconductors during turn-off of the HEXFET's. The value of $R_s$ is small, so at turn-off, most of the current flowing through the HEXFET's is quickly commutated to the snubber circuit. At turn-on, the HEXFET's switch as though the snubber was not present except that they must carry the minute additional current required to discharge $C_s$. The energy stored in $C_s$, while the switches are off is dissipated in $R_s$ at turn-on.

2) Resonant Components: The capacitor in the resonant circuit consists of three series-connected 1-$\mu$F capacitors. This combination gives an equivalent capacitance of 0.33 $\mu$F. The inductance is comprised of the transformer leakage inductance of 3.65 $\mu$H. The resonant frequency $f_r$ is given by (5), and the characteristic impedance of the resonant circuit $Z_0$ is found from (6). Equation (7) shows that the on-time of the switches is equal to 3.45 $\mu$s, or one-half the resonant period. Three hundred nanoseconds of dead time is provided while the inverter switches at the maximum frequency. Thus the maximum switching frequency $f_{max}$ is 133 kHz as given by (8).

$$f_r = \frac{1}{2 \pi \sqrt{LC}} = \frac{1}{2 \pi \sqrt{(3.65 \times 10^{-6})(0.33 \times 10^{-6})}} \approx 145 \text{ kHz}$$

(5)
B. Drive Circuitry for the Switches

One of the most difficult tasks in designing the power section of a switching power supply is designing the drive circuitry for the switches. Even MOSFET's, whose drive requirements are much less stringent than those of bipolar devices, require a drive circuit whose complexity may exceed that of the rest of the power section. For this reason, International Rectifier's IR2110 high-voltage bridge drivers are included in the design of the drive circuitry. The IR2110 requires little external circuitry in driving two insulated gate devices such as MOSFET's or insulated gate bipolar transistors (IGBT's) in a half-bridge configuration [6]. The IR2110 has two independently controlled driver channels. The low-channel input (LIN) controls the low-channel output (LO). The low channel drives the lower device in a half-bridge configuration. The high-channel input (HIN) controls the high-channel output (HO) and drives the upper device in a half-bridge configuration. The shut-down input (SD) disables both outputs regardless of the status of HIN and LIN.

Driving the lower device (S3 or S4 in Fig. 5) in a half-bridge configuration is fairly straightforward, as the source of this device is at the ground potential and remains stable throughout the switching cycle. Driving the upper device (S1 or S2 in Fig. 5), however, presents some difficulty as the source of this device floats between the rail voltage \(V_{BUS}\) and the ground potential throughout the switching cycle. When this device is on, its source voltage is very close to \(V_{BUS}\); therefore, the gate voltage must be driven to a voltage that is greater than \(V_{BUS}\). The IR2110 accomplishes this task by using bootstrapping techniques [6], [7].

Because a full-bridge topology was chosen for the series resonant inverter, two IR2110's are required to drive the four switches. Fig. 6 is a block diagram of the drive circuitry. This figure includes the isolation stage, which isolates the control circuitry from the drivers, the protection stage, which serves to protect the switches, and the driving stage. The control signals are isolated from the IR2110 via Hewlett-Packard HP2211 high-speed logic optocouplers. HIN and LIN are logically coupled to SD through an AND gate. If for some reason both of these signals go high at the same time, then both IR2110's will shut down, turning off all four switches. This measure prevents the catastrophic situation where all of the inverter switches turn on and short-circuit the input rail. In order to operate the inverter as described in the series-resonant inverter section, signal A controls the low channel (LIN) of IR2110 no. 1 and the high channel (HIN) of IR2110 no. 2, and signal B controls HIN of IR2110 no. 1 and LIN of IR2110 no. 2.

C. High-Voltage Transformer

Transformers used in high-frequency applications must be designed carefully in order to minimize their leakage inductances. Furthermore, if the application involves high volt-
ages, then care must also be taken to prevent dielectric breakdown of the insulating material and arcing between turns and windings. Unfortunately, compromises must be made when designing a transformer to operate under both high-frequency and high-voltage conditions. High-frequency design requires a small, high-permeability core, tight windings, and close proximity between primary and secondary. High-voltage design, on the other hand, requires that a minimum separation that depends on the operating voltages and the dielectric breakdown strength of the insulating material be maintained between individual turns and between the primary and secondary windings. The transformer used in this CCPS is wound on a standard toroidal ferrite core with a square cross-section. The primary is wound on top of the secondary with a layer of teflon tape between the two windings for insulation. The turns ratio of the transformer is \(22:275 = 1:12.5\).

**D. Output Stage**

The output stage is a full-bridge rectifier connected to the secondary winding of the high-voltage transformer to provide the charging current for the load capacitor. Each leg of the full-bridge rectifier (shown as a single diode in Fig. 5) consists of three series-connected MUR8100E ultrafast recovery, 1000-V, 8-A diodes. Resistors are connected around each of the diodes to provide voltage division so that each diode is only required to block one-third of the total output voltage. The smoothing inductor \(L_s\) serves to limit the \(di/dt\) of the charging current. This \(di/dt\) limiting provides a smooth charging current.

**E. Feedback and Control Circuitry**

As shown in Fig. 5, the output voltage of the CCPS is resistively divided and fed back to the control circuitry. The feedback circuitry consists of buffers and filters whose main function is to eliminate switching noise from the error signal. The heart of the control circuitry is Unitrode's UC3860 resonant mode power supply controller, which was chosen because of its many useful on-board features [8], [9]. Fig. 7 shows a block diagram of the UC3860.

The variable frequency oscillator (VFO) sets the frequency of control signals A and B. The frequency of the VFO is proportional to the current into the \(I_{\text{VFO}}\) pin and inversely proportional to the capacitance at the \(C_{\text{VFO}}\) pin of the UC3860. The minimum oscillating frequency is programmed by a resistor connected between the precision 5-V reference \(V_{\text{REF}}\) and \(I_{\text{VFO}}\). The oscillator free-running frequency depends on the output of the error amplifier, which modulates the oscillator frequency based on the value of the output voltage of the CCPS. A reference is provided to the noninverting input of the error amplifier \(EA_{\text{IN}}(+)\) by a voltage division of \(V_{\text{REF}}\). Proportional-plus-integral compensation is applied between the inverting input \(EA_{\text{IN}}(-)\) and the output \(EA_{\text{OUT}}\) of the error amplifier to filter switching noise and to provide a fast feedback path. A resistor connected between \(EA_{\text{OUT}}\) and \(I_{\text{VFO}}\) programs the free-running frequency of the VFO. The voltage at \(EA_{\text{OUT}}\) is inversely proportional to the output voltage of the CCPS. Consequently, the current into \(I_{\text{VFO}}\) and, hence, the frequency of the VFO, decrease with increasing output voltage and increase with decreasing output voltage.

The on-time of the one-shot determines the pulse width of the control signals and, thus, the on-time of the inverter switches. The on-time is programmed by a resistor and a capacitor connected in parallel from the RC pin of the UC3860 to ground. At the beginning of each switching cycle, the capacitor is charged and allowed to discharge through the resistor. When the decreasing voltage at the RC pin crosses a threshold, the on-time of the one-shot terminates.

The fault comparator of the UC3860 can be used to disable the outputs of the chip when a fault condition occurs. Situations that are considered fault conditions are defined by the user. In this application, the fault comparator is used as overvoltage protection. Thus a fault condition is defined as the output voltage of the CCPS exceeding the target voltage. A reference is supplied to the inverting input of the fault comparator \(FLT(-)\) by a resistive division of \(V_{\text{REF}}\). The
noninverting input FLT(+) is a signal that is directly proportional to the output voltage of the CCPS. When \( V_{\text{OUT}} \) reaches the target voltage, which corresponds to the end of the charging mode and the beginning of the refresh mode, the UC3860 is disabled by the fault comparator. The fault comparator continues to disable the UC3860 until \( V_{\text{OUT}} \) drops below the target voltage. If the drop in \( V_{\text{OUT}} \) is due to capacitor leakage and parasitic resistances, then the UC3860 momentarily restarts, refreshing the load capacitor with minute bursts of energy. Once the capacitor has been fully refreshed, the fault comparator again disables the control chip. If the drop in \( V_{\text{OUT}} \) is due to the load discharging the capacitor, then the CCPS reenters the charging mode after a short delay.

The undervoltage lockout (UVLO) feature of the UC3860 is normally used to monitor the supply voltage \( V_{\text{CC}} \) when this voltage is derived in an off-line fashion from the CCPS input voltage \( V_{\text{BUS}} \). If \( V_{\text{CC}} \) drops below a certain value, the UVLO will sense this and turn off the UC3860 until \( V_{\text{CC}} \) rises back to its normal voltage. This application, however, uses the UVLO feature for an additional and entirely different purpose. The UVLO is used not only to monitor \( V_{\text{CC}} \) but also to turn off the CCPS while the load discharges the capacitor. This measure keeps the CCPS from supplying the load with additional energy while the capacitor is being discharged.

Although the outputs of the UC3860 can be programmed for several different modes of operation, alternating outputs were chosen for this design to keep the resonant waveforms as symmetric as possible, avoiding transformer core saturation problems. Both outputs are able to source and sink currents up to 3 A peak when charging or discharging a capacitive load such as the gate of a MOSFET. Although the UC3860 is fully capable of directly driving MOSFET's, it does not provide the means to drive MOSFET's with floating sources such as those used as the upper switches in the inverter section of the CCPS. The IR2110's are used for this purpose. The high- and low-voltage levels of the control signals are clamped to \( V_{\text{CC}} \) and ground, respectively, by a Schottky diode array.

The UC3860 has a built-in slow start feature that is implemented by connecting a capacitor between the SFT STRT pin and ground. Upon removal of either a fault or an undervoltage lockout, the slow-start capacitor is charged by an internal current source, and the VFO frequency increases proportionally to the voltage at SFT STRT. So the slow start time is directly proportional to the value of the capacitance at the SFT STRT pin.

### IV. Experimental Results

The performance of the prototype CCPS has been evaluated in the laboratory for both single- and repetitive-charge cases. Energy-storage capacitors having values of 1 and 10 \( \mu \)F were charged to 1500 Vdc by the CCPS and discharged into a dummy load consisting of an overdamped RL circuit and a high-voltage semiconductor switch. Various waveforms were measured with a Tektronix 2440 digitizing oscilloscope and plotted with a Tektronix HC100 plotter. Several of these waveforms are presented and discussed in this section.

Two figures of merit that are useful in analyzing the capacitor-charging capability of the CCPS are its charging and average power output. The charging power is expressed in joules per second and is defined as the time rate of change of energy on the load capacitor during the charging mode. Equation (9) relates the charging power \( P_{\text{CH}} \) to the capacitance of the load capacitor \( C_L \), the target voltage \( V_T \), and the charge time \( t_C \), which is equal to the time spent in the charging mode. The average power \( P_{\text{AV}} \) is expressed in watts and depends on the repetition rate of the load \( f_L \). The expression for the average power output of the CCPS is given in (10).

\[
P_{\text{CH}} = \frac{C_L V_T^2}{2t_C} \quad (\text{J/s}) \quad (9)
\]

\[
P_{\text{AV}} = \frac{1}{2} C_L V_T f_L \quad (\text{W}). \quad (10)
\]

Fig. 8 shows the output voltage of the CCPS, and the two outputs of the UC3860 for a complete charge cycle. For this charge cycle, the load capacitance was 1 \( \mu \)F, and the charge time was approximately 750 \( \mu \)s. Thus, by equation (9), the charging power was

\[
P_{\text{CH}} = \frac{(1 \times 10^{-6})(1500)^2}{2(750 \times 10^{-6})} = 1500 \text{ J/s}.
\]

Refresh pulses from the UC3860 are not visible in this figure because the time scale is too small. The capacitor apparently did not need refreshing until after the oscilloscope had completed its sweep. Fig 9 shows \( V_{\text{ab}} \) and \( I_R \) for a similar charge cycle to that depicted in Fig. 8.

The resonant current during the slow start time, during the time that \( f_s = f_{\text{max}} \) and during the refresh mode, are shown in Fig. 10. The current is discontinuous during part of the slow start time, and, as predicted, it is nearly sinusoidal when \( f = f_{\text{max}} \). Notice that the single current pulse shown for the refresh mode is very small in magnitude, indicating that only a relatively small amount of energy was required to refresh the load capacitor to the target voltage.

Fig. 11 shows \( V_{\text{OUT}} \) while the 1 \( \mu \)F capacitor was charged and discharged at a repetition rate of approximately 800 Hz. The average power output of the CCPS for this repetition rate was

\[
P_{\text{AV}} = \frac{1}{2} (1 \times 10^{-6})(1500)^2(800) = 900 \text{ W}
\]

The output voltage for a single charge cycle with a 10-\( \mu \)F load capacitor is shown in Fig. 12. The charging time for this capacitor was approximately 8 ms. Thus the charging power required during the charging mode was

\[
P_{\text{CH}} = \frac{(10 \times 10^{-6})(1500)^2}{2(8 \times 10^{-3})} = 1400 \text{ J/s}
\]

### V. Conclusions

The power converter discussed in this paper has been shown to be feasible for use as a capacitor-charging power
**Fig. 8.** Output voltage and control signals for a single-charge cycle.

**Fig. 9.** Inverter voltage and resonant current for single-charge cycle.

**Fig. 10.** Resonant current during slow start, while $f = f_{\text{max}}$ and refresh mode.

**Fig. 11.** Output voltage for repetitive charges.
supply. Furthermore, the series-resonant topology and constant on-time control scheme allow zero current switching, which minimizes switching losses and automatic core resetting and reduces the complexity of the high-voltage transformer. In addition, the commercially available integrated circuits used to drive the switches and control the switching sequences require little external circuitry, which minimizes the complexity of the CCPS.

The experimental results presented show that the CCPS is able to charge capacitors ranging from 1–10 μF. A 1-μF capacitor was charged from 0–1500 Vdc in 750 μs, corresponding to a charging power of 1500 J/s. This operation was repeated at a rate of 800 Hz, corresponding to an average power of 900 Watts. A 10-μF capacitor was charged from 0–1500 Vdc in 8 ms.

REFERENCES
[9] Unitrode UC3860 resonant mode power supply controller data sheets, Unitrode Integrated Circuits, Merrimack, NH.