Methods for Determining the Emitter Resistance in SiGe HBTs: A Review and an Evaluation Across Technology Generations

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Abstract—For the experimental determination of the emitter resistance of bipolar junction transistors and HBTs, many methods exist in the literature, which yield quite different results though. In this paper, the most widely used methods are reviewed and applied to SiGe HBTs of different technologies and generations, including different device types (i.e., high-speed and high-voltage transistors). First, the accuracy of the methods is evaluated based on simulated data using a compact model. Explanations for causes of observed inaccuracy or failure are given and discussed. Second, suitable methods are applied to experimental data. In both cases, the results are compared for a large variety of device sizes. This paper and its results provide insight into each method’s accuracy; its application limits with respect to a technology, device size, and operating range; as well as its requirements in terms of equipment and extraction effort. A guideline for extracting the emitter resistance is also given.

Index Terms—Compact modeling, emitter resistance, parameter extraction, SiGe HBT.

I. INTRODUCTION

THE emitter resistance $R_E$ has a significant impact on the high-frequency (HF) performance of bipolar transistors and their corresponding circuits. Its influence increases with advancing technology nodes [1] due to the decreasing emitter size and the lower physical limits of the area-specific resistance components of the emitter stack. As a consequence, many methods have been proposed in the literature that aim at accurately determining the emitter resistance [2]–[32]. The list of references corresponds to a careful selection of the most popular or promising methods that have been reviewed and applied in this paper to SiGe HBTs from a wide variety of process technologies.

There are two fundamentally different approaches for determining the series resistances of a transistor. One approach attempts to extract the resistance directly from measured transistor characteristics after suitably manipulating the terminal parameters and assuming a more or less simplified equivalent circuit (EC). The other approach calculates the resistance from its components based on device geometry and sheet resistances and (area or length) specific contact or interface resistances, which are measured on special test structures. In advanced SiGe HBT technologies, $R_E$ is the only series resistance that cannot be measured with special test structures. In [33] and the literature published thereafter, special Kelvin-type test structures were proposed. Unfortunately, these require the fabrication of an $n^+$ mono-Si emitter layer independently of the poly-Si emitter layer, typically by implantation. Since in modern HBTs the $n^+$ mono-Si emitter is formed by outdiffusion from poly-Si, it is not an independent step anymore. Thus, the fabrication of the structures in [33] has become impossible.

Typically, a method for extracting $R_E$ is applied to the terminal characteristics of a given HBT. The obtained results are then either compared with another method or validated on a selected device characteristic. Unfortunately, this does not prove whether a correct value has been obtained. As will be shown later in this paper, the various methods lead to a large spread in the result of $R_E$ for the same transistor, even if all characteristics have been taken for always the same transistor of the same die and wafer. There are manifold causes for this spread, which will also be discussed in detail.

In general, all methods for determining transistor series resistances assume a more or less simplified EC compared with the one used for circuit simulation and design. Furthermore, each method relies on a particular dc or small-signal characteristic. Therefore, the result for the extracted resistance generally depends on both the assumed EC and the characteristic considered. When inserted into a (production) compact model, the extracted resistance value may give neither the same result for the considered characteristic nor correct results for other device characteristics. This is another reason for using a complete compact model for verifying the actual accuracy of an extraction method.

II. INVESTIGATED PROCESS TECHNOLOGIES

Table I provides an overview of the process technologies the various extraction methods have been applied to and are reported on in this paper. Subsequently, just the process names without the company name will be used. Except for the high-voltage (HV) transistors of B7HF500hv, all other transistors refer to the high-performance version of quite
different process generations and architectures. For each technology, between 6 and 12 widely different emitter sizes have been used as well. This broad range of both HBTs and emitter sizes makes the obtained results representative of the existing and future production process technologies (note that BST, B7HF500, and SG13G2 are prototyping processes).

III. EXTRACTION METHODS AND THEIR VERIFICATION

Since the extraction methods considered in this paper are all based on the measurements directly on a transistor, they can be easily verified by applying them to a compact model. In this paper, HICUM/L2 was employed with a complete set of model parameters that were determined from a geometry scalable extraction procedure using dedicated test structures. For each process technology, the resulting model characteristics were verified over a wide range of bias, frequency, temperature, and device geometry. Capturing the essential features of fabricated transistors with parameters that are believed to be reasonably physics-based is a sufficient condition for the purpose of this paper. The HICUM/L2 model, with its quite sophisticated EC, includes all known physical effects of even the most advanced SiGe HBTs [39], [40]. In contrast, all $R_E$ extraction methods assume a much simpler EC, e.g., the one shown in Fig. 1, which also defines the various elements and variables used later in this paper.

In this section, the basic principle of each extraction method is explained briefly, supported by showing the typical characteristic from which $R_E$ is obtained. The results of each method, applied to the compact model, are then displayed in a single plot for all investigated technologies and compared with the actual value. This provides a quick overview of trends in terms of accuracy. The causes for an observed failure or exceptional agreement will be discussed along with the sensitivity of a method with respect to relevant physical effects and the resulting consequences for selecting the proper bias or frequency range.

Not considered here are methods in which the theory is fundamentally flawed, such as determining $R_E$ from $I_C(V_{BE})$ assuming its low-injection formulation also at high current densities [25], [41]. Furthermore, it was verified by simulation that a current dependence of $R_E$ resulting from current crowding [10] can be safely neglected for the wide range of technologies considered in this paper. As a consequence, the method in [11], which relies on strong emitter current crowding (and also uses two separate base contacts), will not be discussed further for determining $R_E$.

A. $g_m$ Method

Assuming a simple hybrid-$\pi$ EC and including the voltage drop across the emitter series resistance $R_E$ and total base series resistance $R_B$ in the collector (terminal) current formulation yields

$$I_C = I_S \exp \left( \frac{V_{BE} - I_C(R_E + (R_E + R_B)/\beta_t)}{m_C V_T} \right)$$

where $\beta_t = I_C/I_B$ is the external small-signal low-frequency (LF) current gain and $m_C$ is the current-dependent ideality coefficient. The external transconductance $g_m = \partial I_C/\partial V_{BE}|_{V_{BE}}$ can then be written as

$$\frac{1}{g_m} = \frac{m_C V_T}{I_C} + \frac{R_E + R_B}{\beta_t} + \frac{m_C V_T}{\partial I_C/\partial T} \bigg|_{I_C} \frac{\partial V_{BE}}{I_C} \frac{\partial T}{\partial I_C}$$

where the last term represents the impact of a change with temperature (due to self-heating) [19] and the first four terms are valid for constant temperature. Neglecting the last two terms and making $m_C(I_C) = m_{C0} + I_C/I_{mc}$ current-dependent gives the often-used formulation for Si-based transistors

$$\frac{1}{g_m} = \frac{m_{C0} V_T}{I_C} + R_{cor} + \frac{R_B}{\beta_t} + \left( 1 + \frac{1}{\beta_t} \right) R_E$$

where $R_{cor} = V_T/I_{mc}$. Equation (3) was published in [27] (without $R_{cor}$, though) and in a more simplified form (without the last term) in [28]. By plotting the measured $1/g_m$ versus the measured $1/I_C$, the extrapolated intercept on the $y$-axis yields a resistance $R$, from which $R_E$ is obtained after proper correction

$$R_E = \frac{R - [R_{cor} + R_B/\beta_t]}{1 + 1/\beta_t}.$$
B7HF500hv, with the smallest error beyond 50% and 175%, respectively. The method does not work for B7HF500hs and SGB25V, and it increases for SGB25V and B5T to up to 23% and 50%, but due to graded germanium across the BE junction and self-heating is turned OFF, a positive intercept is obtained. The error of the method. Further differences may be caused by the frequency dependence of the small-signal measurements from which $g_m$ is determined.

### B. Extraction From DC Base Current

Ning and Tang [8] proposed a purely dc-based method, in which it is assumed that the observed deviation of the base current $I_B$ from its ideal current $I_{B0}$ is caused solely by the voltage drop across the series resistance

$$I_B = I_{B0} \exp \left( -\frac{I_E R_E + I_B R_B}{m_{BE} V_T} \right)$$

with the base current ideality factor $m_{BE}$. Rearranging (5) gives [8]

$$\frac{m_{BE} V_T}{I_C} \ln \left( \frac{I_{B0}}{I_B} \right) = \left( R_E + \frac{R_{Bi}}{\beta_f} \right) + \frac{R_E + R_{Bx}}{\beta_f}$$

(6)

where $R_B = R_{Bi} + R_{Bx}$ was set ignoring that only the internal base current flows through $R_{Bi}$. The ratio $R_{Bi}/\beta_f$ was included in the first term on the left-hand side, since it was assumed to be (nearly) bias-independent. Plotting $(m_{BE} V_T/I_C) \ln(I_{B0}/I_B)$ versus $1/\beta_f$ gives the $y$-axis intercept $(R_E + R_{Bi}/\beta_f)$ and the slope $R_E + R_{Bx}$. Assuming $R_{Bi}/\beta_f$ to be known allows to determine $R_E$ from the intercept [8].

The method is very sensitive not only to self-heating but also to the extracted ideal base current $I_{B0}$, which should be determined in the vicinity $\beta_f \approx \beta_{f,\text{max}}$.

The application of the method in Fig. 4(a) yields a negative intercept for the respective transistor. In such a case, $R_E$ has to be determined from the slope with known $R_{Bx}$. In contrast, if self-heating is turned OFF, a positive intercept is obtained. The BC barrier effect can also have an impact on the extracted $R_E$ if the $I_B$ increase occurs in the $1/\beta_f$ range that is used for the extrapolation.

The results of applying (6) to different process technologies and emitter sizes are shown in Fig. 5. The best results are obtained for SGB25V, with an error range of $[15, 40] \%$, which tends to increase with emitter area. For BiCMOS7, the error range increases to 20% (smaller size) and 65% (larger size), and it increases further for B7HF500hv and SG13G2, respectively. For BiCMOS7, SGB25V, and SG13G2, significantly too small values have been extracted. For B5T, the results show a very large error spread between 2% and almost 700%. These large errors are observed for larger emitter widths, i.e., smaller $R_E$ values. The method does not work at all for B7HF500hs, with errors $\sim 1000\%$. The reason for this failure is the uncertainty in determining $I_{B0}$ because of the absence of a linear portion in the log($I_B$) characteristic, so that an unambiguous bias range for the extraction cannot be found. The reliability of this extraction method is further reduced (even for a single technology) by the assumptions of: 1) a bias-independent and known term $R_{Bi}/\beta_f$ and 2) the series resistances being the only cause for a
Fig. 4. Example for the extraction method described in [8], applied to a \(0.18 \times 5 \ \mu m^2\) HBT (B5T) (a) with and (b) without self-heating. Reference: \(R_E = 3.76 \ \Omega\).

Fig. 5. Comparison of the results of the Ning–Tang extraction method for different process technologies (same legend as in Fig. 3). \(s\) indicates an extraction from the slope rather than the intercept.

deviation of \(I_B\) from \(I_{B0}\), which may not be the case in double heterojunction bipolar transistor due to the \(BC\) barrier effect. Overall though, the main reason for the observed large errors of this method is self-heating and, in the case of the

failure for the HV process (B7HF500hv), the early onset of high-current effects.

C. Flyback or Open-Collector Method

The flyback method was first published in [2] and later rediscovered twice in [3] and [7]. It attempts to determine \(R_E\) from the current dependence of the external \(CE\) saturation voltage \(V_{CEs} = V_{CE}(I_C = 0)\)

\[
V_{CEs} = V_{CE'\mu} + R_E I_B
\]

which corresponds to a measurement with open collector terminal, i.e., \(I_B = I_E\). In the early publications, a bias-independent internal \(CE\) saturation voltage \(V_{CE's}\) was assumed (according to the Ebers–Moll model). This assumption applies neither to HV transistors with lightly doped collector nor to the modern transistors with spatially dependent collector doping profile and leads to incorrect bias-dependent \(R_E\) values [4], [6]. Thus, in [5] it is proposed to extract \(R_E\) at sufficiently high base currents where the \(V_{CE's}\) current dependence is negligible. However, this can push the operation beyond \(BV_{CEO}\) or to high self-heating and may even lead to the destruction of the transistor. In [18], a complicated subcircuit, including a distributed transistor model, is introduced in order to correct a measured floating voltage curve using a calculated \(V_{CE's}\), while in [6], the bias-dependent \(V_{CE's}(I_B)\) curve is calculated numerically from the SPICE Gummel-Poon model. The most widely used variant of the open-collector method is based on a proposal in [23], in which

\[
V_{CE's} = V_{CE'\mu} \ln \left(1 + \frac{I_B}{I_{CS}}\right)
\]

is expressed by the measured base current and two parameters \(V_{CE'\mu}\) and \(I_{CS}\). The latter depend on the ratio of the electron and hole mobility in the internal collector as well as on the saturation current of the hole transfer current and the hole recombination current of the parasitic pnp transistor, respectively. Together with a bias-independent value of \(R_E\), these two parameters are fitted to the measured \(V_{CE's}(I_B)\) characteristic.

Fig. 6 shows examples for the typically observed curvature of the terminal voltage \(V_{CEs}\) and also the correction voltage \(V_{CE's}\) along with the corresponding fits. The device simulation clearly demonstrates the necessity of the correction as well as the suitability of (8) for describing the curvature. In the mixed-mode device simulation, \(R_E = 3 \ \Omega\) was added externally, while the fitting results in \(R_E = 2.7 \ \Omega\).

Fig. 7 shows the results of this method for different process technologies and emitter sizes. Quite reasonable results with errors not exceeding 20%–25% have been obtained for BiCMOS7, B5T, and B7HF500hs. In these cases, the error distribution is also very narrow, indicating that the method is reliable when it works. However, for SG13G2 and SGB25V, the smallest error is at least 50%. No clear trends with emitter size have been observed. There can be various causes for failure. The analytical expressions given for \(V_{CE's}\) in the literature are all based on a 1-D analysis and ignore the impact of both the BC injection current across the highly
forward biased external BC junction. Also, the analysis in [23] assumes a spatially constant collector doping profile and no BC barrier; hence, it yields only a rough approximation for advanced HBTs. Finally, the current flow through the emitter polysilicon to monosilicon interface is lateral and therefore different from that in a transistor under regular operating conditions, which can cause further errors. However, using a ten-transistor model for the internal transistor, the impact of emitter current crowding on the results was investigated and found to be negligible. This also holds for the impact of self-heating.

D. Low-Frequency Small-Signal Methods

Small-signal methods mostly aim at eliminating the constraint of high injection and the (associated) impact of self-heating. The Z-parameter method was proposed in [42] originally for extracting only the base resistance, but the result for \( Z_{12} \) was then used in [12] for extracting \( R_E \) and was revisited in more detail in [21]. It is based on simplifying the transistor EC to a T-circuit. Then, neglecting the influence of the capacitances yields [12]

\[
\gamma(Z_{12}) \approx \frac{1}{g_m} + R_E. \tag{9}
\]

Plotting \( \gamma(Z_{12}) \), measured at sufficiently low frequency, versus \( 1/I_C \) gives \( R_E \) as y-axis intercept of the extrapolation toward infinite current. In [21], the x-axis was chosen for some reason as \( 1/I_B \), which increases the error by unnecessarily adding the bias dependence of the current gain. Obviously, this method is a simplified form of the \( g_m \) method discussed earlier. Compared with the \( g_m \) method, it suffers, in addition, from the lack of a suitable correction (see \( R_{ce0} \)) and uncertainties resulting from the selection of a “sufficiently” low frequency. Investigations here confirmed that the results are very similar to those of the \( g_m \) method shown in Fig. 3.

Based on a simple hybrid-\( \pi \) EC, \( R_E \) was expressed in [15] by the LF approximations of \( \mathbf{L}_{11} \) and \( \mathbf{L}_{21} \)

\[
R_E = \min \left\{ \frac{-\beta(\mathbf{L}_{11})(1 + x^2) - xr_y}{\beta x_0} \right\} \tag{10}
\]

where \( x = -\beta(\mathbf{L}_{21})/\beta(\mathbf{L}_{11}) \) and \( \beta_0 \) is the LF small-signal current gain. The typical result of the above calculation [Fig. 8(a)] displays a very strong bias dependence, from the minimum of which \( R_E \) is determined. Further analysis shows only for long and narrow emitter fingers (e.g., 0.12 \( \times \) 4.94 \( \mu \text{m}^2 \)) a negligible frequency dependence up to at least peak \( f_t/5 \), which increases to \( \sim 10\% \) for wide emitters (e.g., 0.48 \( \times \) 4.94 \( \mu \text{m}^2 \)).

A similar approach is pursued in [30] based on a significantly more sophisticated EC, which is still simplified though compared with that of production compact models. In [30], an attempt is made to improve \( g_m \) by obtaining a more accurate expression for the internal transconductance \( g_{mi} \). This is accomplished by relating the external small-signal parameters (e.g., \( \mathbf{H} \)) to the internal parameters (e.g., \( \mathbf{Y} \)). After several matrix operations and neglecting terms, \( g_{mi} \) is expressed by the external small-signal parameters and \( R_E \) is calculated from the approximation

\[
R_E = \min \left\{ \frac{\gamma(\mathbf{L}_{11})}{\gamma(\mathbf{L}_{21})} - \gamma \left( \frac{1}{\mathbf{L}_{21}} \right) \right\} \frac{V_T}{m_{BE1}I_B} \tag{11}
\]

with \( I_B \) as the ideal internal base current (i.e., \( m_{BE1} = 1 \)) in [30], \( \mathbf{L}_{11} = (\mathbf{Y}_{11} + \mathbf{Y}_{12})^{-1} \) and \( \mathbf{L}_{21} = (\mathbf{Y}_{21}^{-1} - \mathbf{Y}_{12}^{-1})/(\mathbf{Y}_{11}^{-1} + \mathbf{Y}_{12}^{-1}) \). Plotting the argument in the brackets of (11) versus \( V_{BE} \) [Fig. 8(a)] allows to determine \( R_E \) from the minimum of the obtained curves. In [30], a possible frequency dependence of the terms in (11) is ignored. However, as shown in Fig. 8(b) the right-hand side of (11) can give significantly different results if the frequency is chosen too high.

In [31], a modified version of this method was proposed, which was termed post-deembedding approach because of its analogy to S-parameter deembedding. Its goal was to simplify the derivation and to correct for self-heating as well as the nonideality (\( m_{BE1} > 1 \)) of the internal base current. Applying the version of [31] to the technologies used in this paper yielded lower values for \( R_E \) [Fig. 8(a)] than the
Fig. 8. Typical results for various LF extraction methods applied to B5T. (a) Bias dependence for finding $R_E$ from the minimum value according to method [30], its variant [31], and the method in [15]. (b) Frequency dependence of the method in [30].

This leads to worse accuracy for B5T but to higher accuracy for B7HF500hs.

The results of the methods proposed in [15] [Fig. 9(a)] and in [30] [Fig. 9(b)] are quite similar in their trend for different process technologies and emitter sizes. In general, the method in [30] is more accurate and works more reliably, with the best results being in the 10% error range. A major difference is observed for SGB25V, where the method in [30] fails while that in [15] does not, and for B7HF500hv, where [15] yields much larger errors than [30]. The latter error can be attributed to the early onset of high-current effects which is not taken into account in the derivation of (10). Interestingly, for SGB25V the modified method in [31] gives good results, which is attributed mostly to the self-heating correction. However, the error of the method in [30] can be reduced to <7% for SGB25V if, instead of taking the minimum value, the results are averaged over a certain bias range; the problem though is to find general criteria for the bias range selection. In [29], a method combining dc and LF ac measurements was proposed for extracting $R_E$ from

$$R_E = \frac{\partial V_{BE}}{\partial I_B} \left[ \beta_0 \left( 1 + \frac{\partial \log(\beta_0)}{\partial \log(I_B)} \right) - \frac{\partial I_C}{\partial I_B} \frac{\partial V_{CE}}{\partial I_B} \right]^{-1}. \quad (12)$$

The derivation assumes an ideal internal $I_B(V_{BE})$ characteristic and that self-heating, neutral base recombination, collector impact ionization, and perimeter base current (i.e., the intrinsic current gain equals the extrinsic current gain) are negligible. The derivative $\partial I_B/\partial V_{CE}$ results from the $V_{BC}$ dependence of the internal base resistance. It is suggested that the derivatives of the measured terminal currents with respect to the measured terminal voltages can be calculated from either small-signal LF data or numerically from dc characteristics. Applying the method to the various technologies yielded very large deviations if the derivatives were calculated from dc data. However, if small-signal data are used acceptable results are obtained as shown in Fig. 10. The errors increase with device size and exceed 100% only for SG13G2 and BiCMOS7.
E. Methods Based on Collector Impact Ionization

Expressing the BE terminal voltage by the internal (junction) voltage $V_{BE}$

$$V_{BE} = V_{BE'} + R_E I_E + R_B I_B$$

(13)

allows in principle to determine the series resistances from a simple dc measurement as the difference between $V_{BE}$ and $V_{BE'}$, where the latter can be expressed by (1) through measurable parameters as $V_{BE'} = m_C V_T \ln(I_C/I_S)$. The impact of $R_B$ can be eliminated by forcing $I_B$ to zero with the help of the collector avalanche current. Hence, sweeping $V_{CB}$ so as to find $V_{CB,z} = V_{CB}(I_B = 0)$ yields the measured data pair $(V_{CB,z}, I_{E,z} = I_{C,z})$, from which $R_E$ is determined according to (13) [14]. In the calculation of $V_{BE'}$ from (1), the Early effect is missing, which can make the methods too inaccurate. Including a very simple approximation term, $1 + V_{CB}/V_A$ with $V_A$ as the forward Early voltage, leads to an improved formulation for the emitter resistance [16]

$$R_E = \frac{V_{BE,z} - m_C V_T \ln \left( \frac{I_{E,z}}{I_{S}(1+V_{CB,z}/V_A)} \right)}{I_{E,z}}.$$  (14)

Fig. 11 shows examples for the result obtained for different technologies. Apparently (as also observed in [14]), the extracted value can depend significantly on the bias condition. In [14], the suitable bias range is specified: on the lower limit, the current density has to be high enough to cause a measurable voltage drop across $R_E$. For the upper limit, the onset of high-injection effects in the base was given, which should be replaced by the onset of high injection in the collector. Moreover, although the voltage in Fig. 11 shows a sufficiently wide region with a linear increase with $I_{E,z}$, the curves do not start at zero voltage as would be expected from (14). Fig. 12 shows the results of this method for different process technologies and emitter sizes. All results exhibit a large range of errors between a few percentage points for certain emitter sizes (of BST, SG13G2) and at least 150% and even beyond for other emitter sizes of the same process. There appears to be no correlation between the emitter size and the error. For instance, when sweeping the width at a given length, the error does not follow a trend and also behaves very differently for different widths. The major problems with this method are the requirement for relatively high current densities (in order to generate a measurable voltage drop) and the zero-crossing condition for $I_B$. The latter leads to fairly high $V_{CB}$ values and thus causes significant self-heating. For certain technologies, the necessary $V_{CB}$ value may even be outside the safe operating area, making the method inapplicable. Self-heating increases the error of the method generally, but this degradation of accuracy depends on the amount of $T$ increase for each transistor and process.

F. Combined Extraction of Emitter and Thermal Resistance

Two different methods that extract $R_E$ and $R_{th}$ but follow different approaches are proposed in [22] and [32]. In [22], $I_E R_E$ is expressed by measurable variables from rearranging (5), while $R_{th}$ follows from the calibrated temperature dependence of the base current $I_B$ and the
derivative of the ratio \(I_B(T)/I_B(T_0)\) with respect to the power dissipation \(P_T\). The resulting two equations are linked and, hence, solved iteratively until a consistent set of values for \(R_E\) and \(R_{th}\) is obtained. The method proposed in [32] also uses \(I_B\) as a temperature sensor, but then obtains \(R_E\) from the linear dependence of \(\Delta T = T - T_0\) versus \(V_{CE}\) as shown in Fig. 13. Inserting the output voltage loop into \(\Delta T\) yields \(\Delta T = (V_{CE} - V_{CE,0})I_C R_E\), with \(V_{CE,0} = I_E R_E + I_C R_{Ct}\). The latter is obtained from sweeping \(V_{CE}\) (and thus \(P_T\)) at constant \(I_B\) and then extrapolating the data to \(\Delta T = 0\). Since \(T\) is calculated from \(I_B\) for a given value of \(R_E\), the calculation procedure is iterative (however, it is not necessary to know \(R_{th}\), which is determined simultaneously though).

Fig. 14(a) shows the results of the simultaneous method [22] for different process technologies and emitter sizes. Quite accurate results are obtained, except for the HV process, where the extracted values are far too small. The cause of this error is again the early onset of high-current effects and the resulting reduction of the upper limit of the suitable operating range for extracting \(R_E\) from the slope (Fig. 13).

As shown in Fig. 14(b), the method in [32] yields similar accuracy, including for the HV process. The better results for the latter are attributed to the fact that this method is based on the occurrence of self-heating rather than treating it as an undesired parasitic effect.

G. Small-Signal High-Frequency Methods

The best known approach for determining series resistances from HF characteristics is the circle-impedance method, which appears to have been first proposed in [43]. Over time, various improvements have been proposed [4], [9], [24]. Common to all methods is the assumption of a fairly simple \(\pi\)-EC in order to arrive at reasonably simple analytical expressions for the two-port parameters and thus \(\mathcal{Z}_{11}\). At first order, plotting \(\Re(\mathcal{Z}_{11})\) versus \(\Im(\mathcal{Z}_{11})\) yields a semicircle at not too high frequencies, where distributed and non-quasi-static effects come into play. Neglecting both external parasitic and \(BC\) capacitances, the extrapolation of the semicircle with the real axis toward \(f \to \infty\) yields \(R_B + R_E\). Including the above-mentioned capacitances changes that simple result into one which contains more or less complicated correction terms that depend on the various capacitance components [4], [24] and even the excess phase of the transconductance [4]. Due to the difficulties of determining the correction factors accurately (especially on a single transistor structure) and since \(R_E \ll R_B\), the method has been employed only for determining \(R_B\) but not for \(R_E\) [4], [24]. In [9], \(R_E\) is determined directly from a simplified expression of the input impedance, but again \(R_B\) and the capacitance components need to be known. Fundamentally, the major problem of HF methods is the dependence of the result on the assumed EC. In other words, the extraction results are valid only for the assumed EC.

IV. EXPERIMENTAL RESULTS

Having established the suitability, issues, and limits of the various extraction methods, they were then applied to experimental data. The large amount of results has been
organized such that for each process technology, the extracted $R_E$ from various methods is displayed versus the reciprocal emitter window area, $A_{E0}^{-1}$. Note that RF structures were used for determining $R_E$ on the same devices that were also employed for extracting other model parameters. Due to the lack of space, the representative examples shown in Fig. 15 have been selected. In addition, only those methods that did not exhibit complete failure in Section III were chosen for each technology. This is the reason for showing in Fig. 15(a) the results of only five methods. In all cases, a fairly large spread of the results can be observed, the absolute value of which increases toward smaller emitter sizes (i.e., large $A_{E0}^{-1}$). The data of most methods exhibit quite good straight lines, indicating that the poly/mono interface resistance is the dominating component in $R_E$ with a constant area specific emitter resistivity $\rho_E$ obtained from the slope. Typically, also a positive intercept on the y-axis is obtained, which can be attributed to a probe contact resistance.

1Note that for the same device the measurements for all methods have not always been performed at the same time. Therefore, the probe resistance may vary somewhat.

The results in Fig. 15(a) show a significantly larger spread in the slope than the data in Fig. 15(b)–(d). Of the (in principle) suitable methods for the HV process in Fig. 15(a), the $g_m$ method does not give a straight line at all and the Huszka method shows the completely opposite trend ($R_E$ increases with area). The Tran method yields a fairly small positive slope with the largest standard deviation $\sigma_{\rho_E}$ of the fit to the straight line. Only the Pawlak method gives results with a small $\sigma_{\rho_E}$. However, none of the methods yields similar $R_E$ values for both the HV and high-speed transistor type of B7HF500, which have the same $BE$ structure and thus are expected to have the same value for $\rho_E$.

Despite a quite large spread in absolute resistance, the data in Fig. 15(b) yield similar slopes for all methods, except for the methods in [8] and [15]; also, [8] does not work at all for larger areas (leading to negative $R_E$ values there). In contrast, Fig. 15(c) and (d) shows a relatively small spread in absolute resistance for all methods, except for the Ning–Tang method, which does not seem to yield correct results here either.

The obtained results are summarized in Table II, containing for each method and process the (area specific) emitter resistivity $\rho_E$ and its standard deviation $\sigma_{\rho_E}$, both obtained.
TABLE II

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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SG13G2</td>
<td>3.69</td>
<td>3.10</td>
<td>1.41</td>
<td>4.10</td>
<td>4.18</td>
<td>3.58</td>
<td>3.00</td>
<td>3.43</td>
<td>3.29</td>
<td>3.58</td>
<td></td>
</tr>
<tr>
<td></td>
<td>25.96</td>
<td>41.10</td>
<td>168.40</td>
<td>153.33</td>
<td>86.17</td>
<td>107.53</td>
<td>119.12</td>
<td>25.62</td>
<td>34.33</td>
<td>5.39</td>
<td></td>
</tr>
<tr>
<td>B7</td>
<td>3.48</td>
<td>1.63</td>
<td>1.21</td>
<td>1.70</td>
<td>2.87</td>
<td>3.54</td>
<td>2.20</td>
<td>1.95</td>
<td>2.26</td>
<td>1.63</td>
<td></td>
</tr>
<tr>
<td></td>
<td>75.60</td>
<td>13.15</td>
<td>96.22</td>
<td>51.51</td>
<td>62.87</td>
<td>77.73</td>
<td>53.20</td>
<td>269.06</td>
<td>27.29</td>
<td>13.15</td>
<td></td>
</tr>
<tr>
<td>B7HF500hs</td>
<td>2.05</td>
<td>1.48</td>
<td>4.37</td>
<td>1.53</td>
<td>2.20</td>
<td>3.57</td>
<td>1.83</td>
<td>1.12</td>
<td>2.21</td>
<td>1.90</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7.23</td>
<td>9.00</td>
<td>56.28</td>
<td>18.59</td>
<td>17.60</td>
<td>56.68</td>
<td>2.61</td>
<td>37.69</td>
<td>6.58</td>
<td>3.93</td>
<td></td>
</tr>
<tr>
<td>BicMOS7</td>
<td>14.35</td>
<td>12.59</td>
<td>6.96</td>
<td>24.77</td>
<td>22.00</td>
<td>19.06</td>
<td>9.94</td>
<td>9.93</td>
<td>13.58</td>
<td>13.58</td>
<td></td>
</tr>
<tr>
<td></td>
<td>45.78</td>
<td>39.48</td>
<td>24.77</td>
<td>22.00</td>
<td>19.42</td>
<td>19.94</td>
<td>22.08</td>
<td>21.52</td>
<td>20.68</td>
<td>20.68</td>
<td></td>
</tr>
<tr>
<td>B7HF500hv</td>
<td>8.75</td>
<td>-</td>
<td>0.79</td>
<td>-</td>
<td>0.79</td>
<td>0.79</td>
<td>0.79</td>
<td>0.79</td>
<td>0.79</td>
<td>0.79</td>
<td></td>
</tr>
<tr>
<td>SGB25V</td>
<td>3.85</td>
<td>5.58</td>
<td>2.61</td>
<td>7.04</td>
<td>12.32</td>
<td>4.75</td>
<td>2.96</td>
<td>1.74</td>
<td>5.17</td>
<td>5.17</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.47</td>
<td>4.42</td>
<td>3.30</td>
<td>20.02</td>
<td>12.12</td>
<td>1.81</td>
<td>2.97</td>
<td>4.15</td>
<td>3.27</td>
<td>3.27</td>
<td></td>
</tr>
</tbody>
</table>

2) Determine $\rho_E$ and $\sigma_{\rho_E}$ from fitting a straight line to the $R_E$ versus $1/A_{E0}$ data of each method.

3) Calculate the average value of $\rho_E$ from those methods with lowest $\rho_{Es}$ and use that value during the remaining model parameter extraction (i.e., $R_E = \rho_E/A_{E0}$).

4) Verify the extracted $\rho_E$ by applying the same methods as above to the characteristics generated from the compact model.

The relative standard deviation of $\rho_{Es}$, $\sigma_{\rho_{Es}}$, in the last column of Table II indicates how reliable the results from the proposed extraction method are.

V. CONCLUSION

A comprehensive and detailed study of nine widely used methods (and their variants) for extracting the emitter resistance of bipolar transistors has been presented. The methods have been applied to SiGe HBTs from six different process technologies, ranging from established production to the most advanced prototyping processes. Using also high-performance and HV devices with a wide range of up to 12 emitter sizes, the results of this paper are believed to be representative for the actual accuracy and applicability of the various extraction methods.

It was found that none of the existing methods works reliably across all process technologies. The least reliable method is the one presented in [8], which rarely comes close to the actual value, and those based on HF small-signal measurements, where $R_E$ is masked by the much higher base resistance. Methods based on fly-back/open-collector [2]–[7], [23] and impact ionization [14], [16], which increase the risk of device destruction, are also not reliable in practice. For all methods, the causes for observed failures have been investigated and explained, providing guidance toward their successful usage. The most important causes for deviations are the strongly simplified EC and neglect of important physical effects (such as high-injection, CB barrier effect, and self-heating) in the derivation of the methods. A concise summary of the major cause(s) for failure for each method from fitting the respective data to a straight line. This provides a clear quantitative overview on both the results of each method and the average resistivity $\bar{\rho}_E$ (see second last column in Table II) across all methods for a given process. Here, the spread $\sigma_{\rho_E}$ of the $\rho_E$ calculation is an indication for the consistency of the obtained $\rho_E$ for a given technology.

Overall, the results of the theoretical (i.e., model-based) investigations have been confirmed experimentally. In particular, the various methods behave differently for different process versions. Furthermore, although one can usually find two methods giving similar results, this does not provide proof of the validity of a method. Thus, the recommendation for obtaining the emitter resistance reasonably accurately is as follows.

1) Apply several methods that appear to be most suitable according to the theoretical results.

The relative standard deviation of $\rho_{Es}$, $\sigma_{\rho_{Es}}$, in the last column of Table II indicates how reliable the results from the proposed extraction method are.
method is given in Table III. Similar results have been obtained for InP HBTs [44].

Based on the understanding gained in this paper, a procedure to more reliably determine the emitter resistance is provided. Applying this procedure and the most suitable methods to the wide range of process technologies shows the trend of decreasing emitter resistivity from ~13 Ω·μm² in former processes to ~3 Ω·μm² in advanced processes.

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REFERENCES


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