A 13-dB IIP3 Improved Low-Power CMOS RF Programmable Gain Amplifier Using Differential Circuit Transconductance Linearization for Various Terrestrial Mobile D-TV Applications

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Abstract—A CMOS RF digitally programmable gain amplifier (RF PGA), covering various terrestrial mobile digital TV standards (DMB, ISDB-T, and DVB-H) is implemented as a part of a low-IF tuner IC using 0.18-μm CMOS technology. An improvement of 13-dB IIP3 is attained without significant degradation of other performance criteria like gain, noise figure, common-mode rejection ratio, etc., at similar power consumption. This is achieved by applying a newly proposed differential circuit $g_m''$ (the second derivatives of transconductance) cancellation technique, called the differential multiple gated transistor (DMGTR). In the DMGTR amplifier, the negative value of $g_m''$ in the fully differential amplifier can be compensated by the positive value of $g_m''$ in the pseudo differential amplifier which is properly sized and biased. By adopting the DMGTR, a low-power highly linear RF PGA is implemented. Also, in order to have wide gain range with fine step resolution, a new RF PGA architecture is proposed. The measurement results of the proposed RF PGA exhibit 50-dB gain range with 0.25-dB resolution, 4.5-dB noise figure, a 4-dBm IIP3 (maximum 30 dBm) and 25-dB gain at 16-mW power consumption.

Index Terms—CMOS, digital TV, DMGTR, $g_m''$ cancellation technique, IIP3, linearization, RF programmable gain amplifier.

I. INTRODUCTION

THE INCREASING interest in watching TV in a mobile environment makes it necessary to integrate TV on small hand-held devices, such as mobile phones or personal digital assistants. Terrestrial D-TV standards include Terrestrial-Digital Multimedia Broadcasting (T-DMB) [1] in Korea, Integrated Service Digital Broadcasting-Terrestrial (ISDB-T) [2] in Japan, and Digital Video Broadcasting-Handheld (DVB-H) [3] in Europe. The terrestrial D-TV system can reuse the analog TV transmission system, thus, it can save the money for infrastructure. Table I summarizes various terrestrial mobile digital TV standards. The T-DMB in Korea is evolved from DAB (Digital Audio Broadcasting, Eureka-147) in Europe which has only audio broadcasting. T-DMB has almost the same PHY and MAC layers as the DAB, and T-DMB adds video broadcasting. As shown in Table I, the terrestrial transmission system uses both VHF and UHF bands. Thus, it is better to cover all frequency bands for various market purposes.

Traditional TV tuners, which are not appropriate for a mobile device, consume too much power and also use too many off-chip components and chips because they have limitless power supply and large area. Thus, in order to integrate TV into a mobile device, power consumption and size should be reduced dramatically. System On a Chip (SOC), which integrates all of the functions including the digital part into a single chip, can be the best solution for those requirements. For these reasons, CMOS is believed to be the most promising technology for mobile tuner ICs, with low cost and also SOC capability with digital circuits.

In the integration of tuner front-ends with CMOS for SOC, there exist several stringent requirements, such as immunity to digital circuitry noise [4] and power consumption. The power consumption that is directly related to linearity should be minimized in order to extend the battery time which is more problematic in a mobile device. Thus, it is important to have a high rejection to digital circuitry noise, and maximize linearity/power consumption. Also, a large gain range with fine resolution and a low noise figure (NF) in an RF domain, are still challenging on a single CMOS substrate [5].

In order to maximize linearity/power, a linearity improvement technique should be employed [6]. Previous linearity improvement techniques for CMOS, described in [6] and [7], were only for single-ended topology, which is not appropriate for SOC because of its bad common-mode noise rejection. Also, differential circuit linearity improvement techniques, described
in [8] and [9] are for a pseudo-differential amplifier-based circuit. This is also weak for common-mode noise disturbances which will be discussed later. The other technique [10] consumes too much power and is weak for mismatches.

Another issue in tuner design is the capability to cope with varying power interferers. The best way to deal with those interferers is to give adequate attenuation with fine resolution in RF domain. In this regard, large gain range with fine resolution RF digitally programmable gain amplifier (RF PGA) is required in tuner.

In this paper, we propose a CMOS RF PGA for various terrestrial D-TV standards as a part of the low-IF tuner IC shown in Fig. 1 [11], [12]. This receiver employs a passive-type image rejection mixer [12] for linearity and noise performance. There are several benefits of using passive mixers in direct conversion or low-IF receiver. First, I/f noise is quite relaxed and high linearity can be achievable. However, in this architecture, the linearity burden is squeezed into preceding blocks, in this case, RF PGA. Thus, here we propose a new differential circuit linearity improvement technique, called the differential multiple gated transistor (DMGTR) [13], in order to obtain a low-power highly linear RF PGA. This technique does not lose other performance or consume extra power. Section II introduces the DMGTR technique starting from investigating basic differential circuits behaviors such as current and its first, second, and third derivatives. Section III describes the RF PGA architecture, which is designed to provide wide gain range with fine resolution in wide bandwidth. Section IV presents the experimental
II. DMGTR AMPLIFIER

A differential topology is one of the best ways to reject digital circuitry noise, which usually acts as common-mode disturbance in a SOC [14]. There are two kinds of differential circuits. One is a fully differential amplifier (FDA) and the other is a pseudo-differential amplifier (PDA). Fig. 2 shows the FDA and its current. Two branch currents meet at the center of the $I-V$ curve. Fig. 3 shows the PDA and its current. In this case, the intersection point of two branch currents depends on bias voltage.

results of the DMGTR amplifier and the RF PGA, and the paper concludes in Section V.
It is better for the SOC to use the FDA, which has a higher common-mode noise rejection than the PDA. Because the FDA has a well-defined current source which acts as large feedback impedance over the common-mode signal, while ground over differential signals [14]. Reference [15] compares the linearity between the FDA and the PDA, but the simplified equation cannot give us enough insight into the linearity. Here, we start to investigate the linearity characteristics of the FDA and the PDA with its detailed behaviors of current and then propose a new differential circuit linearity improvement technique.

The FDA’s differential current \([I_+ - (I_-)]\), and the first, second, and third derivative (\(g_{m}, g_{m}',\) and \(g_{m}''\)) of differential current over differential input voltage \(V_{\text{diff}}(V_+ - (V_-))\) are shown in Fig. 4. In this simulation, BSIM 4 v.4 model and commercial simulation tool are used. As is widely known, \(g_{m}''\) is a major dominant factor for third-order nonlinearity (IIP3) in CMOS RF amplifiers [6], [7]. Thus, the negative excursion of \(g_{m}''\) from zero in the FDA degrades IIP3.

The PDA’s differential current and \(g_{m}, g_{m}',\) and \(g_{m}''\) of the differential current of the PDA are shown in Fig. 5. It shows behaviors similar to those of the FDA.
The major difference between the FDA and the PDA lies in $g_{m''}$. Fig. 6 shows $g_{m''}$ behaviors of the FDA. Both a high bias and a low bias case are compared. In the FDA, the negative value of $g_{m''}$ cannot be moved to positive value by changing the bias condition, as shown in Fig. 6(a) and (b). In the case of the PDA, however, it can be moved to positive value by changing the bias voltage, as shown in Fig. 7(a) and (b). Because in the FDA, two branch currents ($I_+, I_-$) always meet at the center of the $I-V$ curve irrespective of the bias condition of tail current source, as shown in Fig. 6. While in the PDA, those two currents can meet at any point, depending on the bias voltage, as shown in Fig. 7. That means in the PDA, the negative value of $g_{m''}$ of the differential current can be moved to a positive value by changing the bias voltage from saturation to near threshold regime. From the above consideration, the negative value of $g_{m''}$ which degrades linearity in the FDA can be compensated with a positive value of $g_{m''}$ in the PDA by adjusting the bias and transistor size of the PDA. This method does not require extra power consumption, as the PDA for compensating $g_{m''}$ is biased at near threshold voltage regime. Here, we propose a new high linearity differential amplifier, the DMGTR amplifier, using the FDA as the main amplifier and the PDA as the auxiliary amplifier. Because most of the signal is amplified by the main amplifier, the benefit of differential circuits, like high common-mode rejection ratio (CMRR), is still maintained. Also, the RF characteristics, like NF and gain, are not degraded in the proposed amplifier. Fig. 8 shows the DMGTR amplifier and $g_{m''}$ linearization by the proposed method. The transistor size of the FDA is 35 $\mu$m/0.18 $\mu$m and the PDA is 60 $\mu$m/0.18 $\mu$m. The current of main amplifier is 1.5 mA and the PDA current is around 70 $\mu$A. The linearization window is wide enough to cover possible mass production variations such as process, temperature, and supply voltage. The bias circuitry for the DMGTR amplifier is shown Fig. 9(a). A conventional current mirror bias circuit is enough for the DMGTR.
amplifier. Even though the PDA is biased at the weak inversion region, the current mirror bias circuit ensures stable operation as discussed in [6]. As the CMOS modeling of derivatives of transconductance is not perfect, it is better to control bias current with digital control bits as shown Fig. 9(b). In this design, the main amplifier is assigned three control bits and the auxiliary amplifier is assigned five control bits for possible mismatches between simulation and real measurement. By changing control bits, the bias current increases or decreases monotonically.

III. RF PGA ARCHITECTURE

To cover a wide gain range with fine resolution in the RF PGA, gain attenuation is divided into four parts, as shown in Fig. 10. A 13-bit gain control word is directly assigned to the RF PGA, and it is composed of a linear 50-dB gain range with 0.25-dB resolution. In the first stage, to attain a large gain range, a resistive attenuator is used. Previous variable gain amplifiers have used a single amplifier with switches [16] or multiple amplifiers without switches [5], [17]. The first one requires an input switch even at the highest gain mode, which results in degradation of the NF. The second one suffers from bandwidth limitation, because of the multi-amplifier configuration. Thus, we find a compromise between both structures using only two amplifiers. Here, we separate the high gain mode amplifier from the low gain mode amplifier, using the same amplifier, and with the switch moved back after the amplifier as shown in the resistive attenuator block of Fig. 10. This resistive attenuator has 8-dB gain step and total 40-dB attenuation. Those first-stage amplifiers also perform single-to-differential conversion, thus removing the off-chip transformer. This is achieved by combining common-source (CS) and common-gate (CG) amplifiers, as shown in the first amplifier of Fig. 11. The CS amplifier in the Fig. 11 amplifies the input signal to the inverted output signal, while the CG amplifies the input signal with the same phase. Thus, we can obtain single-to-differential conversion. The inductor in Fig. 11 is used as the current source of the CG amplifier. Because both the high gain mode and low gain mode use the same amplifier, as shown in Fig. 10, the switch is used to select each amplifier according to gain control. Also, the common-gate amplifier provides 50-Ω input impedance over a wide frequency band. The DMGTR amplifier is used at the second-stage amplifier, which determines the overall RF PGA linearity. The first and second amplifiers have a digitally controlled gain range, to cover the previous gain step, using load impedance switching. The first-stage amplifier covers 12 dB with 4-dB step, and the second amplifier covers 4 dB with 1-dB step. In order to deliver the signal effectively to the next stage, the third-stage amplifier employs a source-follower. The source-follower step-gain amplifier [18] covers 1 dB with 0.25-dB step.

IV. MEASUREMENT RESULT

A. DMGTR Amplifier

The photograph of the evaluation board of the DMGTR amplifier and RF PGA is shown in Fig. 12. A 4:1 transformer is used to convert the differential signal output to a single-ended signal, for the measurement equipment. Fig. 13 shows the measurement result of A two-tone intermodulation test of the conventional FDA and the DMGTR amplifier. An on-chip source-follower buffer amplifier is used at the output of the FDA and the DMGTR amplifiers for measurement. The input power level is −25 dBm and the frequency is around 500 MHz. With a similar fundamental power, the DMGTR decreases the third-order intermodulation distortion (IMD3) power up to 26 dB, and the corresponding IIP3 improvement is 13 dB. As a result, the FDA shows IIP3 of −3 dBm at 2.8-mA current consumption, while the DMGTR amplifier shows IIP3 of 10 dBm at 2.9-mA current consumption. The NF is 5.7 dB for both the FDA and
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Fig. 13. Measurement result of two-tone intermodulation test. The conventional FDA and the proposed DMGTR amplifier are compared. Measured frequency is 500 MHz.

Fig. 14. DMGTR IIP3 measurement result versus auxiliary amplifier bias, showing wide linearization window. Measured frequency is 500 MHz.

Fig. 15. Die photo of proposed RF PGA.

Fig. 16. Gain range measurement result of the proposed RF PGA, covering 50 dB with 0.25-dB resolution seamlessly. Measured frequency is 670 MHz.

Fig. 17. IIP3 Measurement of the proposed RF PGA. Measured frequency is 500 MHz.

Table II shows the comparison between previous wideband amplifiers and the DMGTR amplifier.

### Table II

<table>
<thead>
<tr>
<th></th>
<th>Frequency (GHz)</th>
<th>IIP3 (dBm)</th>
<th>NF (dB)</th>
<th>Gain (dB)</th>
<th>Technology</th>
<th>Power (mW) @ supply voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[19]</td>
<td>0.25-1.1</td>
<td>-12.5</td>
<td>2</td>
<td>13.7</td>
<td>0.25um CMOS</td>
<td>35@2.5</td>
</tr>
<tr>
<td>[20]</td>
<td>0.42-1.18</td>
<td>-14.2</td>
<td>2.3</td>
<td>24</td>
<td>0.4um CMOS</td>
<td>35@2.7</td>
</tr>
<tr>
<td>[21]</td>
<td>3.2-4.8</td>
<td>-12.5</td>
<td>2.3</td>
<td>24</td>
<td>0.18 um CMOS</td>
<td>20@2.5</td>
</tr>
<tr>
<td>Conventional</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>FDA</td>
<td>0.47-0.86</td>
<td>-3</td>
<td>5.7</td>
<td>10</td>
<td>0.18 um CMOS</td>
<td>5@1.8</td>
</tr>
<tr>
<td>This Work</td>
<td>0.47-0.86</td>
<td>10</td>
<td>5.7</td>
<td>10</td>
<td>0.18 um CMOS</td>
<td>5.2@1.8</td>
</tr>
</tbody>
</table>

**B. RF PGA**

Fig. 15 shows the die photograph of the proposed RF PGA. Both the VHF and UHF RF PGAs are implemented using 0.18-μm one-poly six-metal (1P 6M) CMOS process and occupies a die area of 0.52 mm² (excluding pads). All pins are...
TABLE III
PERFORMANCE SUMMARY OF RF PGAS

<table>
<thead>
<tr>
<th>Band</th>
<th>Standard (Frequency, MHz)</th>
<th>Gain (dB)</th>
<th>NF (dB)</th>
<th>IIP3 (dBm)</th>
<th>Gain range (dB)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VHF</td>
<td>DAB/DMB (174–245) ISDB-T 3seg. (190–220)</td>
<td>28</td>
<td>3.0</td>
<td>-5</td>
<td>50</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td>ISDB-T 1seg. (470–770) DVB-H (450–860)</td>
<td>25</td>
<td>4.5</td>
<td>-4</td>
<td>50</td>
<td>16</td>
</tr>
</tbody>
</table>

This work, 0.18μm CMOS

TABLE IV
PERFORMANCE COMPARISON OF LOW-POWER RF VARIABLE GAIN AMPLIFIERS

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>IIP3 (dBm)</th>
<th>NF (dB)</th>
<th>Gain/ Gain range (mWatt)</th>
<th>Technology</th>
<th>Power consumption (mWatt/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[17] 470–770</td>
<td>-14</td>
<td>2.7</td>
<td>19/60</td>
<td>SiGe BiCMOS</td>
<td>25.23</td>
</tr>
<tr>
<td>[22] 54–860</td>
<td>5/11 dB</td>
<td>6</td>
<td>22/12</td>
<td>0.18um CMOS</td>
<td>41.4/1.8</td>
</tr>
<tr>
<td>[23] 48–860</td>
<td>21.25</td>
<td>6</td>
<td>6/12</td>
<td>0.5um BiCMOS</td>
<td>NA/3.3</td>
</tr>
<tr>
<td>This work</td>
<td>-4</td>
<td>4.5</td>
<td>25/50</td>
<td>0.18um CMOS</td>
<td>16/1.8</td>
</tr>
</tbody>
</table>

E SD-protected using the PN diode. As the common-gate and common-source amplifier in the first-stage amplifier provides 50-Ω input impedance, S11 is under −10 dB over the entire frequency band. Fig. 16 shows the full range gain step of 670 MHz. The gain step covers a total of 50-dB gain range seamlessly with 0.25-dB resolution. Fig. 17 shows the IIP3 measurement result of the proposed RF PGA. Table III shows the measurement summary of the VHF and UHF RF PGAs. The NF of the UHF RF PGA is 4.5 dB, its voltage gain is 25 dB, and its IIP3 is −4 dBm at 16 mW. In the lowest gain mode, IIP3 reaches +30 dBm. A comparison with previous works is shown in Table IV. This work shows 10 dB higher IIP3 at even much lower power consumption (65%) than previous work [17], even though that work was implemented by bipolar in SiGe BiCMOS technology.

V. CONCLUSION

A new differential circuit linearity improvement technique, DMGTR, is newly proposed, based on analysis of the characteristics of differential current and its derivatives of the FDA and the PDA, and verified with measurement. Measurement results of the DMGTR amplifier show maximum 13-dB improvement of IIP3 without sacrificing other characteristics such as gain, NF, and CMRR with wide linearization window. Also, this method does not require extra power consumption.

Employing the DMGTR, a low-power, low-noise, and highly linear RF PGA for terrestrial D-TV applications is designed and measured. Also, to cover a wide gain range with fine step resolution over a wide frequency range, new gain control methods are proposed and verified by measurement. The fabricated RF PGA shows 50-dB gain range with 0.25-dB resolution, 4.5-dB NF, a −4-dBm IIP3, and voltage gain of 25 dB at 16–06mW power consumption.

ACKNOWLEDGMENT

The authors would like to thank Prof. K. Lee, Dr. B. K. Ko, Dr. B. Kim, Mr. Y. Cho, and Mr. S. Kim for technical discussion, and Mr. T. Lee for layout support.

REFERENCES


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