Real-Time External Compensation of Threshold Voltage Shift Using Double-Gate Oxide TFTs in a Gate Driving System

Bong-Hyun You, Soo-Yeon Lee, Seok-Ha Hong, Jae-Hoon Lee, Hyun-Chang Kim, Student Member, IEEE, Ha-Ram Ju, Student Member, IEEE, Moon-Chul Choi, Student Member, IEEE, and Deog-Kyoon Jeong, Senior Member, IEEE

Abstract—In order to suppress the malfunction caused by the shift of the threshold voltage ($V_{TH}$) of oxide thin film transistors (TFTs) to a negative value, double-gate TFTs are used in the shift register of the gate driving system to control $V_{TH}$ by adjusting the top gate bias. The proposed circuit detects the current consumption of the shift register and adjusts $V_{TH}$ so that the current consumption of the shift register is regulated within the desired value. The system includes a compensation algorithm, which can search for an optimized top gate bias in various circumstances such as process fluctuations and ambient temperature change. The proposed system provides a stable operation compared with a conventional structure especially at high temperature. Experimental results show that, in the conventional system without compensation, the output voltage of the shift register deteriorates at 80°C and above, and the power consumption increases from 1.15 to 2.14 mW after 21600 s of continuous operation at 60°C. On the other hand, the proposed system provides a stable gate output up to 100°C and keeps the power consumption below 1.10 mW by adjusting the top gate bias responding to environment changes.

Index Terms—Double-gate thin-film transistor (TFT), oxide TFT, shift register.

I. INTRODUCTION

INTEGRATION of shift register circuits on the glass panel offers the advantage of low thickness, light weight, and low cost owing to the reduction in the number of ICs used in the display panel [1]–[3]. Therefore, many shift register circuits employing n-type thin film transistors (TFTs), such as a-Si:H and oxide TFTs, have been reported [4]–[13]. In particular, oxide TFTs attracted much attention due to high mobility and good uniformity [14]. However, oxide TFTs often shows a negative threshold voltage ($V_{TH}$) because of their sensitivity to process fluctuation, temperature, and electrical stress [15]–[17]. The gate-source voltage ($V_{GS}$) for turning off the TFTs is usually zero in the circuit operation. However, TFTs with negative $V_{TH}$ cause malfunction and/or high power consumption with a significant leakage current in the OFF condition. To overcome these problems, most studies have focused on the shift register circuit structure suitable for negative $V_{TH}$ devices [8]–[13]. An additional low-voltage source [8]–[11] or double-gate TFTs [12] are employed to turn off the TFTs. As for double-gate TFTs, $V_{TH}$ can be controlled by the top gate bias [18], [19]. $V_{TH}$ of oxide TFTs can have a positive $V_{TH}$ shift when a lower voltage than the source voltage is applied to the top gate.

In this paper, we proposed a new driving system for shift register circuits employing oxide TFTs. The proposed system includes a circuit for sensing the current consumption, a feedback control system to supply the adjusted top gate voltage, and a software algorithm for searching the optimal top gate bias voltage. The system regulates the current consumption of the shift register within the desired value by adjusting $V_{TH}$ above zero through the top gate, thereby produces stable gate driving signals against process fluctuations and harsh temperature conditions.

II. OXIDE TFT CHARACTERISTICS

Fig. 1 shows the transfer curves and $V_{TH}$ of the fabricated oxide TFTs according to the increase of temperature.
the power consumption but also causes the malfunction of the circuit operation. In the shift register circuits composed of TFTs, a bootstrapping node turns on the pull-up TFTs [4]–[12]. The leakage current may discharge the bootstrapping node such that the bootstrapped voltage is reduced, resulting in a degraded gate output voltage.

To overcome the problem of the negative $V_{TH}$ shift of the oxide TFTs, a shift register circuit using a double-gate TFT structure has been proposed [12]. The cross-section of the double-gate TFT is shown in Fig. 2(a). Fig. 2(b) shows the effect of the $V_{TH}$ control on the experimental double-gate oxide TFTs. A detailed fabrication process of single gate and double-gate TFTs is reported in [19]. It should be noted that when the top gate voltage ($V_{TG}$) lower than the source voltage is applied, $V_{TH}$ of the double-gate TFTs changes in the positive direction. In this study, $V_{TH}$ is found to shift linearly by $V_{TG}$ with the ratio of –1.23 V/V.

It is also well-known that $V_{TH}$ of the oxide TFTs shifts towards the negative direction with an increase in temperature. To prevent a negative $V_{TH}$, a negative $V_{TH}$ must be applied in the double-gate TFTs. However, too much $V_{TH}$ shift towards the positive direction decreases the ON current. It is important for the shift register to be able to turn on the gate line during the display operation. Therefore, proper biasing at optimized $V_{TG}$ is essential for the shift register employing double-gate TFTs. In this paper, we propose an external compensation circuit by controlling the top gate bias of the double-gate TFTs for a highly stable operation of the shift register. A prototype chip has been fabricated to verify the functions.

III. PROPOSED COMPENSATION DRIVING

A conventional shift register consists of a Q-node charging TFT, a gate output ($G_{OUT}$) driving TFT, a reset TFT, and pull-down TFTs. The Q-node is charged by the previous output signal and turns on the $G_{OUT}$ driving TFT, passing the clock signal. The reset and pull-down TFTs are required to keep the gate line at a low voltage during the OFF state. In the conventional shift register circuit, power consumption is increased with a negative shift of $V_{TH}$ because the current in the OFF state is increased. Based on the circuit structure [7], we use double-gate TFTs to attain a stable circuit operation.

In order to drive the conventional shift register, a level shifter, digital circuits such as timing controller, and dc power sources such as $V_{ON}$ and $V_{SS}$ are required. The level shifter converts the voltage levels in the digital clock domain to analog levels suitable for the shift register employing double-gate TFTs. Input clocks are CLK for odd stages and CLKB for even stages of the shift register.

We propose an optimal point searching algorithm to decide the top gate voltage. Since the $V_{TH}$ shift changes the leakage current in the shift register, we propose a current sensing system shown in Fig. 3. An optimized top gate voltage is obtained by monitoring the current consumption of the shift register. An analog-to-digital convertor (ADC) converts the sensed value and the feedback voltage level is computed in the algorithm part. Then, the adjusted top gate voltage ($V_{TG}$) in the double-gate TFTs is applied through a digital-to-analog convertor (DAC).

In the current sensing circuit, a voltage drop across $V_{ON}$ is inevitable which affects not only the shift register operation but also the power consumption of the driving system. In the proposed system, a series resister ($R_S$) and a sense amplifier form the current sensing scheme as shown in Fig. 4. The current is sensed via the voltage drop across $R_S$. The amplified voltage ($V_{AMP}$) is converted to current, $I_1$, and it is integrated by the capacitor, $C_1$ after Reset goes low. $V_{INTEG}$ is the result of current integration and is applied to the input of the ADC. Since the shift register consists of TFTs continuously switching ON and OFF by the clock signals, it leads to pulsed dynamic and static currents. To detect not only the dynamic but also the static

![Fig. 2. (a) Cross section of oxide double gate TFT and (b) effect of top gate bias on $V_{TH}$ shift recovery.](image1)

![Fig. 3. (a) Current scheme and (b) structure of the proposed driving system for shift register, where $V_{TG}$ is top gate voltage of double gate TFTs in shift register.](image2)
current, the current integration method is better than sampling the total current at a single moment. Furthermore, it also has the advantage of filtering out the system noise. $I_{OFFSET}$ in Fig. 4 is for compensating the offset current of the V-I converter. The power dissipation of the designed amplifier and the V-I converter are 90 and 36 $\mu$W, respectively.

Fig. 5 shows the timing diagram of the major signals in the proposed system. The STV is the start signal for the shift register connected to the first stage. The signal RESET is for initializing the integrated current from the previous frame during the vertical blank period. When the shift register starts operating with the STV signal, $V_{ADC}$ is increased by current integration as shown in Fig. 5. The rising rate of $V_{ADC}$ depends on $I_{INTEG}$. $I_{INTEG}$ is the time interval for integration and, at the end of $I_{INTEG}$, $V_{ADC}$ is sampled by the ADC as shown in Fig. 6. The ADC input must be sampled well in advance before $V_{ADC}$ is saturated. Therefore, $I_{INTEG}$ should be less than $1.8 \text{ V} \times C_L/I_{MAX}$, where $I_{MAX}$ is the maximum sensing current in the system. Finally, $V_{TG}$ is calculated and forwarded to the shift register during the vertical blank period.

IV. OPTIMAL POINT SEARCHING

The proposed system includes a searching algorithm, which returns an optimum $V_{TG}$ according to the detected current value. The Oxide TFTs are sensitive not only to electrical and temperature stress but also to the process fluctuation. The current consumption differs from glass to glass and the oxide TFT ages as the operation time is increased. In other words, a lookup table for compensation is valid only for a certain condition. The table data should be dynamically changed when $V_{TH}$ is shifted by the electrical stress, temperature stress, and process fluctuation. Therefore, a proper searching algorithm is required to locate the optimized $V_{TG}$ under all operating conditions. Fig. 7 shows a simplified block diagram of the proposed searching algorithm. It is designed to find the $V_{TG}$ that induces a minimum current consumption. Among the various techniques for finding the minimum value, a golden section search method is adopted due to its fast process time [20].

The proposed algorithm comprises two steps as shown in Fig. 7. In the first step, a search for an initial boundary range is performed. Narrowing of the boundary range is required because an extremely high or low $V_{TG}$ from the optimum value can cause a malfunction of the shift register. Initially, $V_{TG}$ is set as $V_{SS}$ and the default initial boundary range is $[−2, 2]$. When $V_{TG}$ varies from $−5$ to $5$, the boundary range is limited to $4$. To find out if there is a minimum point within the selected boundary, sensing results at the boundary and at the center are compared. When the sensing results exhibit an increasing or decreasing function, the boundary range is shifted by about $2$. An example of the boundary searching step is illustrated in Fig. 8(a). The next step is to find the minimum value inside the boundary range as shown in Fig. 8(b). In this step, the boundary is narrowed down by comparing the two sensing results at the points away from the upper and lower boundaries by $(1−g) × 4$, where $g$ is the
Fig. 8. Examples of (a) initial boundary searching and (b) minimum point searching process, where g is golden rule ratio with a value of about 0.625.

golden ratio, $g \approx 0.625$. The boundary range is then narrowed by selecting the lower valued point as the new boundary. Then the range is decreased to $g \times 4V$ at the next iteration. The total iteration time ($n$) can be calculated as below

$$6 \leq 256 \cdot g^n. \quad (1)$$

With the 8-bit system, the value 6 in the left-hand side in Inequality (1) indicates the binary value of DAC output of the minimum resolvable boundary range in the last step. The maximum range of 256 is narrowed down by $g$ in each step until the range reaches 6. Thus, $n = 8$ is an adequate number and the minimum value is found in the eighth iteration.

V. RESULTS AND DISCUSSIONS

A 16-stage shift register prototype has been fabricated by employing the inverted staggered etch-back oxide TFTs. The fabricated double-gate TFTs demonstrate a linear shift in $V_{TH}$ with a slope of $-1.23 V/V$ by the top gate-to-source voltage. $V_{TH}$ of the oxide TFTs shifts in the negative direction when the ambient temperature is increased as is shown in [21]. The average current of the 16-stage shift register is measured as $V_{TG}$ is varied. When $V_{TG}$ changes from $-10$ to $10$ V, $I_{VON}$ shows a shape of a valley as shown in Fig. 9. It exhibits the minimum when $V_{TG}$ is $-15$ V. $V_{TG}$ of $-15$ V corresponds to $V_{SS}$ of the system, i.e., $0$ V. Fig. 9 shows the two measured results at the ambient and elevated temperatures. Thus, demonstration of a highly stable gate output voltage is in order with a properly designed feedback system, which compensates the negative $V_{TH}$ shift.

To verify the overall function of the proposed system, a prototype system has been built using commercial ICs, such as ADC0804, DAC0808, mosfet, and FPGA, as shown in Fig. 10. The key parameters of $t_{WAIT}$ and $t_{INTEG}$ shown in Fig. 5 are 5.33 and 1.33 ms, respectively. Using an 8-bit successive approximation ADC, a conversion time $t_{CONV}$ of 0.2 ms is required and added to the overall timing.

Fig. 11 shows the time evolution of power consumption at $60^\circ C$. A power of 1.15 mW at the initial state changes to 2.14 mW after 21600 s in the conventional system whereas the proposed system recorded a stable power consumption of $1.15 \pm 0.08$ mW. The sensed current level is significantly low ($\sim 102 \mu A$) since only 16 stages are used in the shift register, which implies that the fluctuation caused by noise is relatively large. Although there is a fluctuation of about 7% in the compensated power consumption, it does not influence the on/off levels of the gate output. From the measured results, it is confirmed that the proposed system compensates the time-variant $V_{TH}$ shift and improves the performance of the shift register significantly.

Fig. 9. Measured results of $V_{ON}$ current according to top gate voltage ($V_{TG}$) at 16-stage shift register.

Fig. 10. Photograph of an external feedback compensation system.
The gate output characteristics and the power consumption of the conventional and the proposed system are compared as the operating temperature varies. In order to verify the proposed algorithm, we have measured the 14th gate output among 16 stages by increasing the temperature from 25 to 100°C. It is well known that when the temperature of oxide-TFT is increased, $V_{TH}$ of oxide-TFT is decreased. The gate output of the conventional system is degraded at 100°C, while that of the proposed system is maintained at 25°C. The power consumption of the conventional system deteriorates with increasing temperature. The proposed system, on the other hand, maintains the minimum current consumption under various ambient temperatures.

In a manufactured product, the panel is operated over the back light unit, which raises the operating temperature and incurs stress on the oxide TFTs in the shift registers of the driving system on the panel. The light can be blocked in the shift register area; however, the increase of temperature is inevitable. From the experimental results, it seems that the temperature is the dominant cause of the $V_{TH}$ shift even though most of the TFTs in the shift register suffer from the AC bias stress.

VI. CONCLUSION

In this paper, we propose a new driving system of the shift register employing oxide TFTs. The system senses an increase in current consumption caused by the $V_{TH}$ shift and compensates it by applying the top gate bias in the double-gate TFTs in the shift register. The compensation algorithm in the system ensures a long-term, suitable operation for devices employing shift registers with oxide TFTs that are prone to a negative $V_{TH}$ shift under various environmental variations.

REFERENCES

metal-based source–drain contacts in amorphous InGaZnO thin film trans-


2010.

section search in one dimension,” in Numerical Recipes: The Art of Sci-
cientific Computing, 3rd ed. New York, NY, USA: Cambridge Univ. Press,
2007, p. 492.

[21] S.-J. Kim et al., “Effect of channel layer thickness on characteristics and 
stability of amorphous hafnium-indium-zinc oxide thin film transistors,”

Bong-Hyun You received the B.S. degree in electrical engineering from Inha University, Incheon, South Korea, in 1990. He received the M.S. degree in electrical engineering and computer science from Seoul National University, Seoul, South Korea, in 2003, where he is currently working toward the Ph.D. degree.

He is a Vice President of Samsung Display Gyunggi-do, South Korea. His earlier accomplishments included the development of larger size LCD TVs. He has been in charge of advanced product development for TV, digital information display, notebook and monitor applications including high-end LCD module schemes and special purpose display of next generation technology such as internal touch-screen panel, three-dimensional vision, ultra-high definition resolution, and high frame rate driving. He has also published more than 11 papers in journals and international conference proceeding.

Soo-Yeon Lee received the B.S. and Ph.D. degrees from the Department of Electrical and Computer Engineering, Seoul National University, Seoul, South Korea, in 2009 and 2013, respectively.

She has been a Senior Engineer of Samsung Display Gyunggi-do, South Korea, since 2013. Her research interest includes the driving system of liquid crystal display.

Moon-Chul Choi (S’15) received the B.S. degree in electrical and electronics engineering from Chung Ang University, Seoul, South Korea, in 2013. He is currently working toward the Ph.D. degree in electrical engineering at Seoul National University, Seoul, South Korea.

His research interests include integrated circuits for silicon photonics and high-speed I/O circuits.

Seok-Ha Hong received the B.S. and M.S. degrees from the Department of Electrical and Computer Engineering, Hanyang University, Seoul, South Korea, in 2008 and 2010, respectively.

He is currently a Senior Engineer of Samsung Display Gyunggi-do, South Korea, from 2010. His research interests include the display driving system design and architecture of advanced display technology.

Ha-Ram Ju (S’14) received the B.S. degree in electrical engineering and computer science from Seoul National University, Seoul, South Korea, in 2013, where he is currently working toward the Ph.D. degree.

His research interests include high-speed I/O interfaces, optical links, and power management ICs.

Jae-Hoon Lee received the Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 2007.

He is currently a Principal Engineer at Samsung Display, Gyunggi-do, South Korea, in the Driving Development Group, in charge of the architecture of advanced display product. His specific R&D activities and accomplishments include the integrated circuit design on the glass substrate, for AMLCDs and AMOLEDs. In the AMLCD area, he developed the low power and highly reliable amorphous silicon gate driver circuit for the mass production. Also, he developed the pixel circuit for AMOLED. For the past three years, his R&D efforts are focused on the AM OLED TV, and highly advanced LCD product. He has more than 70 publications and 50 patents on display technology.

Deog-Kyoon Jeong (S’85–M’89–SM’09) received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, South Korea, in 1981 and 1984, respectively, and the Ph.D. degree in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA, in 1989.

From 1989 to 1991, he was with Texas Instruments, Dallas, TX, USA, as a Member of the Technical Staff and worked on the modeling and design of BiCMOS gates and the single-chip implementation of the SPARC architecture. Then, he joined the faculty of the Department of Electronics Engineering and Inter-University Semiconductor Research Center, Seoul National University, Seoul, South Korea, where he is currently a Professor. He is one of the cofounders of Silicon Image, which specializes in digital interface circuits for video displays such as DVI and HDMI. His main research interests include the design of high-speed I/O circuits, phase-locked loops, and network switch architectures.

Dr. Jeong received the ISSCC Takuo Sugano Award in 2005 for Outstanding Far-East Paper.
学霸图书馆

www.xuebalib.com

本文献由“学霸图书馆-文献云下载”收集自网络，仅供学习交流使用。

学霸图书馆（www.xuebalib.com）是一个“整合众多图书馆数据库资源，提供一站式文献检索和下载服务”的24小时在线不限IP图书馆。

图书馆致力于便利、促进学习与科研，提供最强文献下载服务。

图书馆导航：

图书馆首页 文献云下载 图书馆入口 外文数据库大全 疑难文献辅助工具