A 65 nm CMOS - Stacked Folded Fully Differential (SFFD) PA Structure for W-CDMA Application

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Abstract— This paper presents a 65nm CMOS-power amplifier (PA) designed for mobile communications. The PA is based on a new structure, the Stacked Folded Fully Differential (SFFD) which is inspired by a push-pull structure. The PA is designed for the UMTS W-CDMA standard which requires linearity from -20 dBm to 24 dBm output power. The power amplifier provides 31 dBm output power with 26% of power added efficiency (PAE) at 1.95 GHz. The linear gain is 20 dB and the compression point (OCP1) is 25.6 dBm. In order to meet the UMTS W-CDMA requirements, the PA is linear until 24dBm, which is the maximum output power required by this standard.

I. INTRODUCTION

The diversity of wireless communications has grown over the recent years. Modern generations of wireless communications’ applications imply new standards and impose ever higher requirements in terms of performance. The design of WWAN (Wireless Wide Area Network) or WMAN (Wireless Metropolitan Area Network) application with a low cost technology is very difficult to achieve and is also a real challenge [1].

The technological miniaturization allows a higher density of integration, which is an advantage for a fully integrated transceiver system. But we have to deal with this constraint to fulfill specifications of wireless standard: reach high output power with low gate width technology. Two main physics phenomena related to the miniaturization cause obstacles in the fully integrated CMOS design and limit the performance of a power amplifier: the reduction of the breakdown voltage and the reduction of the substrate resistivity. The first effect limits the output power and the second one reduces the power efficiency of the amplifier. Furthermore, this technological miniaturization degrades the linearity-communication distance trade-off. The W-CDMA standard belongs to WWAN which requires a long distance communication increasing the difficulty to obtain a linear amplification.

This paper illustrates the use of the SFFD structure to obtain a high output power with a low cost and low gate width CMOS technology. To highlight the difficulty of this work, we propose a state of the art about the influence of the technological reduction in the power amplifier performance. When we decrease the technological size, we must reduce the supply voltage to preserve the components. But this reduction leads to a diminution of the output power at 1dB compression point (OCP1) and the PAE. As an example, the maximum output power is 23, 23, 19.5 and 23 dBm in [3], [4], [5], [6] respectively, which is not sufficient to fulfill the W-CDMA specifications. To meet this standard, one PA must provide an OCP1 of 27 dBm. Moreover, we can see that PAE is lower when gate size decrease, so we must take really care of PAE in 65 nm technology since PAE is very important issue in PA design.

II. INFLUENCE OF TECHNOLOGICAL REDUCTION

A. State of the art

TABLE I presents a comparison between several recent published papers about PAs designed in CMOS technology [3], [4], [5] and [6].

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>CMOS 0.25µm</td>
<td>CMOS 0.18µm</td>
<td>CMOS 0.18µm</td>
<td>CMOS 0.13µm</td>
</tr>
<tr>
<td>Freq (GHz)</td>
<td>2.4</td>
<td>2.4</td>
<td>5.2</td>
<td>2.45</td>
</tr>
<tr>
<td>Supply voltage (V)</td>
<td>2.5</td>
<td>2.4</td>
<td>1.8</td>
<td>1.8</td>
</tr>
<tr>
<td>Pout (dBm)</td>
<td>Max: 23 P1dB: 21 Spec: 20</td>
<td>Max: 23 P1dB: 21 Spec: 20</td>
<td>Max: 19.5 P1dB: 16 Spec: NC</td>
<td>Max: 23 P1dB: NC Spec: NC</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>18.8</td>
<td>35.5</td>
<td>15</td>
<td>-</td>
</tr>
<tr>
<td>PAE (%)</td>
<td>Max: 45 18@20dBm</td>
<td>Max: 42 15@20dBm</td>
<td>Max: 32 13@P1dB</td>
<td>Max: 30</td>
</tr>
<tr>
<td>Standard</td>
<td>ISM band</td>
<td>Bluetooth</td>
<td>WLAN</td>
<td>Bluetooth</td>
</tr>
<tr>
<td>Architecture</td>
<td>Common source</td>
<td>Cascade</td>
<td>Push-Pull (PA/)</td>
<td></td>
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</table>

When we decrease the technological size, we must reduce the supply voltage to preserve the components. But this reduction leads to a diminution of the output power at 1dB compression point (OCP1) and the PAE. As an example, the maximum output power is 23, 23, 19.5 and 23 dBm in [3], [4], [5], [6] respectively, which is not sufficient to fulfill the W-CDMA specifications. To meet this standard, one PA must provide an OCP1 of 27 dBm. Moreover, we can see that PAE is lower when gate size decrease, so we must take really care of PAE in 65 nm technology since PAE is very important issue in PA design.

978-1-4244-2182-4/08/$25.00 ©2008 IEEE.
B. UMTS standard requirement

UMTS W-CDMA standard belongs to WWAN. Figure 1. presents the WWAN situation in wireless communication.

![Figure 1. Data rate according to distance communication.](image)

The WWAN requires a long distance communication and a medium data rate, with a minimum consumption. Thereof, the UMTS standard requires a high linearity to preserve the information carried by the signal envelope (since a non constant envelope modulation is used: HPSK) in order to optimize the data transfer. This standard also requires a huge output power to obtain a long distance communication.

Thus, the PA must respond to several challenges. Power challenge and linearity challenge, in order to obtain respectively a high output power with low cost technology and a good linearity-efficiency trade-off. Finally, we want to design a new structure in order to obtain a good linearity-gain trade off. To meet UMTS W-CDMA requirements, the PA remains linear until 24dBm, which is the maximum output power required by this standard. For this reason, the OCP1 must be at least 27dBm in order to preserve a linear amplification.

To design this PA with a low cost technology, it was necessary to develop new architectures. Indeed, the technology limitation increases the difficulty to obtain such level of output power.

C. PA Architecture

The overall PA structure is shown in Figure 2. Two gain stages compose the PA: the Driver stage and the Power stage. They are designed respectively to reach a high gain and the desired output power. Figure 3. illustrates the topology of the Driver stage and Power stage, with a different size component.

![Figure 2. PA Topology](image)

The circuit impedance matching is 50Ω. The capacitors C1, C2, C3 and the inductors L1 and L2 are dedicated to the input and the interstage impedance matching.

Most of the PAs are designed with a common source structure [9], [10]. When the supply voltage decreases, the cascode solution replaces the usual designs [5]. For lower gate widths, a Push-Pull structure is more suitable [4]. We propose to use a new structure, the Stacked Folded Fully Differential (SFFD) PA to increase the supply voltage and to have a higher power gain. This structure is described in section III.

D. Bonding

The bondings connected to the PA output degrade strongly the impedance matching and hence the system performances. Indeed, a bonding is equivalent to a self in series with a resistance when based on a simplified electrical model. Moreover, the output impedance is lower when the output power increases. Since the bondings have a strong influence on the output characteristic, their effects have been taken into account in the design and during simulations.

III. STACKED FOLDED FULLY DIFFERENTIAL PA DESIGN

This section describes the design of the SFFD PA according to the criteria presented in the first part of this paper. The circuit has been designed in the 65 nm CMOS technology from STMicroelectronics.

A. PA design and equations system

A simplified topology of the SFFD PA stage is presented in Figure 3. The capacitors C1 and C2 are coupling capacitances for the input signal. The bonding effect is used for the drain degeneration of the transistors. The input power is applied to the two stacked transistors (M1 and M2) with no need of a particular phase shifting between the two cascode transistors. In addition, the M1 and M2 gates are connected to the same equivalent impedance.

Rather than using traditional differential structure where output power is limited by the breakdown voltage of transistors (M2, M2’), we add in stacked a new differential pair of transistors (M1, M1’). This solution allows to increase the total output excursion in comparison with traditional differential pair. However, this structure decreases lightly the gain, but increases the linearity system. Hereafter, we present equations of SFFDS.
\[ V_{DS,M1} = \left( A_{1\text{min}} + \frac{A_{1\text{max}} - A_{1\text{min}}}{2} \right) + \left( \frac{A_{1\text{max}} - A_{1\text{min}}}{2} \right) \cos \omega t \]

\[ V_{DS,M2} = \left( A_{2\text{min}} + \frac{A_{2\text{max}} - A_{2\text{min}}}{2} \right) + \left( \frac{A_{2\text{max}} - A_{2\text{min}}}{2} \right) \cos \omega t \]

\[ V'_{DS,M1} = \left( A_{1\text{max}} + \frac{A_{1\text{max}} - A_{1\text{min}}}{2} \right) - \left( \frac{A_{1\text{max}} - A_{1\text{min}}}{2} \right) \cos \omega t \]

\[ V'_{DS,M2} = \left( A_{2\text{max}} + \frac{A_{2\text{max}} - A_{2\text{min}}}{2} \right) - \left( \frac{A_{2\text{max}} - A_{2\text{min}}}{2} \right) \cos \omega t \]

We obtain the output voltage with:

\[ V_{Out} = \left( A_{1\text{max}} - A_{1\text{min}} \right) \cos \omega t + \left( A_{2\text{max}} - A_{2\text{min}} \right) \cos \omega t \]

The additional pair of transistor (M1 and M1') allows to increase the total output voltage excursion.

B. Relevance of this design

Figure 4. presents half SFFD circuit and associated \( V_{DS}(t) \). To allow a different biasing and excursion, transistors M1 and M2 are not obligated to have the same gate thickness. Indeed, when the two transistors are not differently biased, transistor M2 will always be off and this structure will not correctly work. It implies that \( Bias1 \) must be greater than \( Bias2 \). Transistor M1 can have a thicker gate oxide than transistor M2 in order to sustain higher voltage. For example, transistor M1 can be biased in class AB and transistor M2 in class B. The biasing class allows an output power modulation. One of the transistors can also use a dynamic biasing to increase the linearity.

C. Schematic simulation result

The CW simulation of this structure was performed with Cadence RF spectrum. It has shown that the PA offers a maximum output power of 31dBm and a power of 26dBm at OCP1. The PA is therefore sufficiently linear and gives a high power. The simulation allowed to validate the operating principle of the structure.

IV. LAYOUT OF THE PA

The circuit is designed to be implemented in a 65 nm CMOS technology from STMicroelectronics which provides 8 metal layers, high voltage transistors and MIM capacitors. Figure 5. presents the layout of the PA. The passive components must take a large silicon area to obtain a high output power. Nevertheless, it increases the system consumption and thus decreases the PAE. The bias current must be around 600 mA and the lines must be optimised to respect the 27 dBm output power at 1dB compression point conditions (in order to be linear at 24 dBm) at high temperatures under 2 V supply voltage. The width of the higher lines is superior to 50µm which increases considerably the size of the circuit.

The power amplifier has an equivalent output impedance of 5 \( \Omega \), which is the condition for an optimal gain and linearity. Overall, the chip size remains small, with an area of 0.672 mm² without pads (60% occupied by the passive components and lines). The 5 \( \Omega \) to 50 \( \Omega \) matching networks is realized off-chip, in order to avoid the implementation of a strongly passive component and to increase the die size and the cost of the process.

V. POST LAYOUT SIMULATION RESULTS

A. Post Layout Simulation

The SFFDS has been simulated using Cadence Spectre RF. Under CW conditions and to be as realistic as possible, the simulations were carried out at the temperature of 90°C.

The simulation results are presented in Figure 6. At 1.95 GHz, the maximum gain is 20 dB for an isolation of -43 dB.
The maximum output power ($P_{\text{out max}}$) and the output power at 1 dB compression point (OCP1dB) are 31 dBm and 25.6 dBm respectively. This system is considered particularly linear between -20 dBm and 24 dBm output power. The PAE is 25% at $P_{\text{out max}}$, 10% at P1dB, and 7% at 24 dBm output power (maximal power specified by the UMTS W-CDMA standard). At 1.95 GHz, the simulations results give a S11 of -33 dB and a S22 of -7.2 dB. Thanks to UMTS W-CDMA standard). At 1.95 GHz, the simulations results are composed with the ones found in the literature.

The previous results are composed with the ones found in the literature.

The design feasibility of a PA dedicated to UMTS W-CDMA standard in 65 nm CMOS technology has been demonstrated in this paper. This power amplifier uses a new structure, Stacked Folded Fully Differential, and provides 31 dBm maximal output power with PAE of 25% at 1.95 GHz. It also provides a good isolation of -43 dB allowing a maximum gain (20 dB). The system is matched at 50 Ω. The OCP1dB is 25.6 dBm and hence the amplification is linear at 24 dBm, the maximum output power specified by the standard. In comparison, this work shows 31 dBm output power with a low cost technology whereas the reference [11] exhibits only 19.5 dBm. The structure proposed respond to the UMTS W-CDMA standard using a low width CMOS technology. It enables strong density of integration for transceivers systems by reducing the chip area. The PA is the main energy consumer within the transmitter [12]. Therefore, to preserve battery life time which is major of importance in mobile application, it’s very important to increase the PAE. Works are underway on improving the gain and the PAE.

### REFERENCES


The comparison emphasizes the capability of this structure to provide high output power. However these performances, in terms of output power and linearity, are possible at the price of PAE degradation.
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