Design Considerations of Soft-Switched Buck PFC Converter With Constant On-Time (COT) Control

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Abstract—In contrast to the conventional boost power factor correction (PFC) converter, the buck PFC converter can achieve high efficiency in the entire universal input voltage range. A critical conduction mode (CRM) soft-switched buck PFC converter with constant on-time control is presented in this paper. The design methodology and criteria for zero-voltage switching range, high efficiency and low harmonics of the CRM buck ac–dc converter are achieved. A 100-W prototype built up according to the proposed design criteria shows that the input current harmonics meet the IEC61000-3-2 (Class D) standard and the efficiency is higher than 0.965 during the universal input range.

Index Terms—AC–DC, buck power factor correction (PFC), high efficiency, zero-voltage switching (ZVS).

I. INTRODUCTION

WITH the development of power electronics technology, many power converters that use capacitor-input filter have resulted in severe harmonic contamination. In order to reduce the harmonic current, IEC61000-3-2 has forced the ac/dc converters to meet the limits imposed by [1]. At present, power factor correction (PFC) is a good method to provide an almost sinusoidal input current. The boost converter is the most popular PFC topology, because the input current can be easily shaped and tracks the input voltage. However, in universal input condition, the boost PFC cannot achieve high efficiency at low line because it works with large duty cycle in order to get high-voltage conversion gain with 90-V ac input and 400-V dc output. Generally speaking, the maximum power dissipation at low line determines the minimum required heat sinker. Therefore, it is hard to increases the power density of boost PFC converter attributes to the thermal problem at low line, especially for adapter application. With bridgeless structure for boost PFC converter [2]–[4], the efficiency can be improved at low line. But, more components should be added to deal with the electromagnetic interference (EMI) issue [5], which leads to high cost.

Discontinuous conduction mode/continuous-conduction mode (CCM) boundary control [6] or variable duty cycle control [7] for boost converter can also improve the efficiency at low line. But, it is still difficult to achieve efficiency higher than 96% for PFC stage at low-power application. Using the buck converter as a PFC preregulator has been introduced in [8]–[20]. The drawbacks of the universal-line boost PFC converter can be overcome by a buck ac–dc converter, which suffers from a distorted input current but may meet the limits imposed by IEC61000-3-2 criteria [15]. But, hard switching causes additional EMI noise and switching loss especially at high input [8]–[18].

The literature [15], [18] proposed a clamped-current buck PFC. The buck inductor works in the CCM around the peak value of the line voltage, which causes reverse-recovery losses in diode. Some control strategies are proposed in [19] and [20], these control strategies cannot still achieve soft switching for buck converters. Therefore, the switching loss increases with the increase of input voltage and switching frequency. The resonant zero-voltage switching (ZVS) techniques for the buck dc–dc converter have been investigated in [21]–[27]. With additional passive or active components, ZVS can be achieved very well [23]–[27]. But, more components increase the complexity and cost of the circuit. With the quasi-square wave technique [23], the ZVS is achieved easily. But the control logic will be very difficult because the duty cycle is variable in PFC application. The critical-conduction-mode (CRM) buck dc–dc converter can eliminate the reverse-recovery loss in the diode, and achieve zero-voltage turn ON for switch [21], [28]. A CRM Buck PFC converter with constant on-time (COT) control is proposed in [29] and [30] as shown in Fig. 1. Although the switching period is variable, the on time of one switching cycle of the switch is almost constant in one line cycle because the
bandwidth of error amplifier is much lower than line frequency and its output $V_{EAO}$ is almost constant. Hence, the peak current in the switch is almost in proportional to the input voltage, if output is assumed constant during one whole line cycle because the output capacitance $C_o$ is large enough. But, there are dead zones in the input current because when the input is lower than output $V_o$, the converter does not work. More detailed principle analysis and verifications of COT controlled ZVS buck PFC converter is introduced in this paper. In order to demonstrate the principle of the buck PFC converter with COT control, Fig. 2 shows the simplified currents in switch and input terminal corresponding to the input voltage during half line cycle.

II. PRINCIPLE OF COT CONTROLLED CRM BUCK PFC

A. Brief Description of the Control Scheme

The buck converter operates in CRM may eliminate the diode reverse-recovery losses, and provide its advantage for ZVS for the turn ON of the switch if the input voltage is lower than double of the output voltage.

In order to demonstrate the COT control principle and soft switching performance of the proposed buck PFC converter, Fig. 3 shows the key waveforms in one switching cycle according to simplified control schematic in Fig. 1. When load and input are constant, the on time of the switch is fixed, which is determined by comparing the constant-slope ramp $V_{ramp}$ and $V_{EAO}$. When switch is ON, inductor current increases linearly and the slope is determined by the difference between input and output voltage and the inductance. Thus, the peak current value is a function of the input voltage as described in (1). Accordingly, the peak current in working region can follow the input voltage, when output voltage $V_o$ is constant

$$\frac{V_{in} - V_o}{L}T_{on} = I_P.$$  

When $S$ is turned OFF, current in inductor begins decreasing and $V_{ds}$ increases rapidly because the inductor current charge the intrinsic capacitors very fast. When the inductor current drops to zero, it is detected by a detecting circuit. At the same time, a resonant interval caused by the intrinsic capacitor and inductor $L$ appears. The voltage $V_{ds}$ decreases due to this resonance and the inductor current reverses a little. And after a certain time delay $t_D$, the switch $S$ is turned ON. With the decrease of $V_{ds}$, the switching ON losses of $S$ and the reverse recovery in diode $D$ can be reduced significantly. With certain input and output range, ZVS turn ON for $S$ can be achieved. Also, this COT control scheme for CRM buck PFC has its advantage of simple circuit implementation without analog multiplier.

B. ZVS Operating Principle for PFC Converter

Although the input of PFC converter is sinusoidal source, ZVS characteristics of buck PFC converter can still be analyzed with dc input because the switching frequency is much higher than the line frequency; the input can be seen as a constant voltage source during the switching cycle. Fig. 4 is the simplified equivalent dc–dc circuit of COT CRM Buck PFC converter. The intrinsic capacitors of
switch and diode are assumed to be $C_S$ and $C_D$, respectively. In order to analyze, the ZVS range and condition, the operating period in one switching cycle of the buck converter is divided into four stages. Fig. 5 shows the equivalent circuits of the converter modes during one switching cycle. It is assumed that input is higher than output and it works in step-down mode. And, the switching OFF transition period is omitted because of its little effect on the designing process.

Stage 1 ($t_0$ to $t_1$): At $t_0$, $S$ is ON and the inductor $L$ is charged by voltage ($V_{in}$,$V_o$). Then, the current $i_L$ increases linearly with the slope ($V_{in} − V_o$)/$L$, the current $i_S$ in switch $S$ equals to inductor current $i_L$ during this interval. According to (1), when $V_o$ is constant, the peak value of $i_S$ is proportional to $V_{in}$. Hence, the peak input current of buck converter is also in proportion to $V_{in}$. As shown in Fig. 3, $v_{ramp}$ begins increasing at $t_0$, and this interval ends when $v_{ramp}$ reaches $V_{EAO}$. The equivalent circuit of this interval is shown in Fig. 5(a).

Stage 2 ($t_1$ to $t_2$): At $t_1$, the voltage $v_{ramp}$ reaches $V_{EAO}$, and $S$ turns OFF. Because the inductor current is at peak value, the intrinsic capacitors are charged to $V_{in}$ very fast. Hence, this interval is much less than the half resonant period between the inductor and the intrinsic capacitors. Also, the current $i_L$ almost does not change. Hence, the inductor can be simplified as a current source during this interval, and the intrinsic capacitors are charged by a constant current source. When the voltage $v_{ds}$ is charged to $V_o$, diode $D$ begins conducting. The equivalent circuit of this mode is shown in Fig. 5(b).

Stage 3 ($t_2$ to $t_3$): After the conducting of diode $D$, the inductor $L$ is discharged by $V_o$. The equivalent circuit is shown in Fig. 5(c). This stage ends when current $i_D$ decrease to zero.

Stage 4 ($t_3$ to $t_4$): At $t_3$, when $i_D$ is zero, the inductor $L$ begins to resonates with capacitors $C_D$ and $C_S$. Because the initial current value of inductor $L$ is zero, the ZVS turn ON is dependent on the resonant parameters and initial value of capacitor voltage. Therefore, this transition period cannot be simplified because it influences the ZVS characteristics. As the inductor $L$ resonates with the capacitors, the voltage $v_{ds}$ decreases from $V_{in}$.

According to (1), the minimum value of $v_{ds}$ appears at half resonant period. Therefore, if $V_{in}$ is lower than two times of $V_o$, ZVS can be achieved easily.

$$i_L(t) = \frac{(V_{in} - V_o)}{Zr} \sin \omega \cdot (t - t_2) - \frac{v_{ds}(t_2)}{Zr} \sin \omega \cdot (t - t_2)$$

$$= -\frac{V_o}{Zr} \sin \omega \cdot (t - t_2)$$

where

$$Zr = \sqrt{L/(C_S + C_D)}, \quad \omega = \frac{1}{\sqrt{L(C_S + C_D)}}$$

(2)

This stage ends when $S$ turns ON, and a new switching cycle begins. In order to simplify the analysis, the switching transition intervals (Stage 2 and Stage 4) are neglected in following steady-state analysis.

C. Input Current Analysis

Based on the switching cycle analysis, the operating principles and characteristics as a PFC converter can be derived. When the input voltage is lower than the output voltage in half line cycle, the buck converter does not work. As shown in Fig. 2, the conduction angle of the input current equals $(\pi - 2\theta_0)$. Assuming $V_{im}$ is the amplitude of the line voltage, then, angle $\theta_0$ is defined as $\theta_0 = \arcsin(V_o/V_{im})$.

When the input voltage is higher than the output voltage, the buck converter begins working, and the slope of the inductor current $i_L$ meets the (1) for the working region in half line cycle

$$L \frac{di_L(t)}{dt} = V_{im} \sin(\theta) - V_o, \quad \theta \in (\theta_0, \pi - \theta_0)$$

(5)

where $\theta = \omega t$ and $\omega = 2\pi \cdot fL$ is the line angular frequency.

So, the peak value of the input current during switching cycle in (1) can be modified as follows:

$$I_p(\theta) = \frac{V_{im} \sin(\theta)}{L} - \frac{V_o}{L} T_{on}$$

(6)
where \( T_{on} \) is the on-time of the switch, which is almost constant during half line cycle. Since the buck converter operates in CRM during the entire conducting angle, the duty cycle can be obtained as follows:

\[
D(\theta) = \frac{V_o}{V_{in}|\sin(\theta)|}, \quad \theta \in (\theta_o, \pi - \theta_o).
\]  

(7)

Then, the average input current \( i_{av} \) of the buck converter is determined as follows:

\[
i_{av}(\theta) = \frac{I_{on}(\theta)D(\theta)}{2}, \quad \theta \in (\theta_o, \pi - \theta_o).
\]

(8)

By substituting (6) and (7) into (8), the final expression for the input current is obtained as follows:

\[
i_{av}(\theta) = \begin{cases} \frac{V_{in} \sin(\theta) - V_o}{2L} T_{on} \frac{V_o}{V_{in} \sin(\theta)}, & \theta \in (\theta_o, \pi - \theta_o), \\ 0, & \text{otherwise}. \end{cases}
\]

(9)

The input current contains only odd harmonics, whose rms value can be calculated from (10) by Fourier analysis

\[
I_{2k+1} = \frac{2\sqrt{2}}{\pi} \int_{0}^{\pi/2} \frac{(V_{in}|\sin(\theta)| - V_o) \cdot T_{on}}{2L} \cdot \frac{V_o}{V_{in}|\sin(\theta)|} \cdot \sin((2k + 1) \cdot \theta) d\theta
\]

where \( k \) is a natural number.

It can be seen that the harmonics is affected not only by \( V_{in} \), but also by \( V_o \).

According to (9), the rms value of the input current is defined as follows:

\[
I_{in,\text{rms}} = \sqrt{\frac{2}{\pi} \int_{0}^{\pi/2} \left( \frac{V_{in}|\sin(\theta)| - V_o \cdot T_{on}}{2L} \cdot \frac{V_o}{V_{in}|\sin(\theta)|} \right)^2 d\theta}
\]

(11)

Hence, the input power factor (PF) is obtained as follows:

\[
PF = \frac{P_{in}}{V_{in,\text{rms}} I_{in,\text{rms}}}
\]

(12)

where \( V_{in,\text{rms}} = V_{in}/\sqrt{2} \), and the total harmonic distortion (THD) is obtained as follows:

\[
\text{THD} = \sqrt{\cos^2(\phi)} \frac{PF^2}{PF^2 - 1}
\]

(13)

where the phase shift angle \( \phi \) is assumed to be zero.

From the aforementioned analysis, the equations for the input current harmonics and PF are derived based on the operating principles, which are useful in designing a buck PFC converter.

III. DESIGN OF COT CRM BUCK PFC

In this section, the design of the CRM buck PFC is based on the previous analysis, and it focuses on the selections of output voltage and inductance. The mathematical modal derived in the previous section is used for designing a 100-W buck PFC with universal input voltage (\( V_{in,\text{rms}} = 90–264 \text{ V}_{ac} \)), which is used as the front end in a laptop adapter.

A. Output Voltage Selection

For energy star introduced a new PF legislation of 0.9 at full load, it is necessary to design the buck PFC maintaining the power factor over 0.9 at normalized low line (115 V_{ac}) and normalized high line (230 V_{ac}), respectively. Within a half line cycle, the input current can flow only when the input voltage is greater than the output voltage. It should be noted that the PF is affected by the output voltage significantly.

Fig. 7 shows the calculated curve of PF as the function of output voltage at 115-V_{rms} input. It can be concluded that with an increasing output voltage, the PF decreases. Theoretical calculation results show that the PF could maintain greater than 0.9 only if the output voltage is set less than 105 V. Although lower output results in higher PF, the efficiency of buck converter will decrease with the decrease of output voltage at same load. Also, because the possible voltage rating of electrolytic capacitor near to 105 V is 100 V, the output voltage is preferred to be set around 90 V considering the voltage stress of the output capacitor.

B. Buck Inductance Selection

After the output voltage is determined, the key design variable is the buck inductance \( L \). The input power \( P_{in} \) is calculated as follows:

\[
P_{in} = \frac{2}{\pi} \int_{0}^{\pi/2} i_{av}(\theta) V_{in} |\sin(\theta)| d\theta.
\]

(14)

Assuming \( \eta \) is the efficiency of the converter, the output power \( P_o \) can be expressed as follows:

\[
P_o = \eta P_{in} = \frac{2\eta}{\pi} \int_{0}^{\pi/2} i_{av}(\theta) V_{in} |\sin(\theta)| d\theta.
\]

(15)

By substituting (9) into (15), the expression is modified as follows:

\[
P_o = \frac{\eta T_{on}}{\pi L} \int_{0}^{\pi/2} (V_{in}|\sin(\theta)| - V_o) V_o d\theta
\]

(16)
T_{off}(\theta) = \frac{I_p(\theta) \cdot L}{V_o}.
\tag{17}

Combining (6) and (17), we can get the switching frequency function
\[ f_s(\theta) = \frac{1}{T_{on} + T_{off}(\theta)} = \frac{V_o}{T_{on} \cdot V_{im} \sin(\theta)}. \tag{18} \]

Obviously, the lowest frequency in half line cycle appears at \( \theta = \pi/2 \).

From (16), \( T_{on} \) can be expressed as follows:
\[ T_{on} = \frac{\pi \cdot L \cdot P_o}{\frac{\eta}{\sqrt{2}} \cdot \int_{\theta_0}^{\pi/2} (V_{im} |\sin(\theta)| - V_o) \cdot d\theta}. \tag{19} \]

Combining (18) and (19), it is obtained that
\[ f_s = \frac{\eta \cdot V_o^2}{\pi \cdot L \cdot P_o \cdot V_{im} |\sin(\theta)|} \int_{\theta_0}^{\pi/2} (V_{im} |\sin(\theta)| - V_o) \cdot d\theta, \]
\[ \theta_0 \leq \theta \leq \pi - \theta_0. \tag{20} \]

Obviously, the minimum switching frequency appears at full load because the off time and on time increase with load increase. Therefore, the minimum frequency as a function of input voltage \( V_{im} \) can be obtained when \( \theta = \pi/2 \)
\[ f_{s_{\text{min}}}(V_{im,\text{rms}}) = \frac{\eta \cdot V_o^2}{\pi \cdot L \cdot P_o \cdot V_{im,\text{rms}} \cdot \sqrt{2}} \int_{\theta_0}^{\pi/2} (V_{im,\text{rms}} |\sin(\theta)| - V_o) \cdot d\theta. \tag{21} \]

According to (21), the switching frequency at the peak point of input voltage is plotted in Fig. 8 at different rms value of input voltage.

Then, the inductance \( L \) is obtained as follows:
\[ L = \frac{\eta \cdot V_o^2}{\pi \cdot f_{s_{\text{min}}} \cdot P_o \cdot V_{im,\text{min}} \int_{\theta_0}^{\pi/2} (V_{im,\text{min}} |\sin(\theta)| - V_o) \cdot d\theta} \tag{22} \]

where \( V_{im,\text{min}} = 90 \).

If the minimum switching frequency \( f_{s_{\text{min}}} \) is assumed to be 25 kHz and the output voltage is designed at 90 V, the inductance is obtained as \( L = 150 \mu H \). Fig. 9 shows the calculated switching frequency versus different input voltages (90, 170, 265 V_{ac}) as the function of the phase angle. It is evident that the minimum switching frequency occurs at the peak of the 90 V_{ac} input, which is close to 25 kHz.

Based on (9) and the parameters designed earlier, the input average current waveforms at 115 and 230 V_{ac} input can be calculated and the curves are shown in Fig. 10. Since the buck converter does not shape the line current around the zero crossing of the line voltage, it will cause a current distortion.

IV. EXPERIMENTAL VERIFICATIONS

According to the design considerations of the previous sections, a 100-W COT controlled CRM buck PFC prototype was built up with universal input and 90-V_{dc} output. The control IC is NCP1607 from Onsemi, which is a commercial PFC controller with constant on time. Fig. 11 shows the schematics of the COT controlled buck PFC prototype and the corresponding design parameters are listed in it. The photo of the prototype is shown in Fig. 12.

The measured input voltage and input current waveforms at nominal low line (115 V_{ac}) and nominal high line (230 V_{ac}) are presented in Fig. 13(a) and (b), which are in a good agreement with the calculated waveforms in Fig. 10. The currents in switch and diode in one switching cycle are shown in Fig. 14. There is no reverse current in diode due to the boundary current mode (BCM) operating at low line in Fig. 14 (a). Even at high line, valley switching almost eliminates the reverse-recovery loss in Fig. 14(b). The measured MOSFET drain-source voltage \( V_{ds} \) and gate driving voltage \( V_{gs} \) at nominal low line (115 V_{ac}) and

![Fig. 8. Minimum switching frequency in function of \( V_{im,\text{rms}} \) at different inductance (\( P_o = 100 \) W, efficiency \( \eta \) is assumed to be 0.96).](image1)

![Fig. 9. Calculated switching frequency versus different input voltage.](image2)

![Fig. 10. Calculated input average current waveforms of 100 W CRM Buck PFC at different input voltage (\( L = 150 \mu H, V_o = 90 \) V).](image3)
nominal high line (230 V\textsubscript{ac}) are presented in Fig. 15(a) and (b), respectively. From previous analysis, for 90-V output, ZVS can be achieved when $V_{\text{in}}$ is lower than 180 V. It can be seen that ZVS is achieved during whole line cycle at low-line input because the peak voltage of input is still lower than 180 V. At high line, ZVS is lost when input voltage is higher than 180 V. However, valley switching is also achieved for high input. Therefore, the switching on loss and the reverse-recovery loss of diode are both minimized.

Regarding the harmonic content of the line current, the measured results are shown in Fig. 16 together with the limits of IEC61000-3-2 Class D standard and the calculated results by (10). The experimental results verify the theoretical expectations very well except for the third component, which is much lower in calculated results than measurement. It is caused by the input filter capacitor, which causes an additional phase shift and is not considered in the calculation of (10). The harmonics of the input current waveforms is increased by the additional phase shift, but it still meets the standard with a large margin.

In order to verify the influence of output voltage, efficiencies and PF results at full load are measured with different output voltages showed in Figs. 17 and 18, respectively. It can be concluded that the circuit efficiency is significantly affected by the output voltage, and with an increasing of output voltage, the PF decrease. In order to make a tradeoff between efficiency and PF, 90-V output is an optimum design point. It can be seen in Fig. 17 that the CRM buck PFC maintains efficiency higher than
0.965 across the entire line voltage range. The losses of common mode filter and control circuit are not included in the efficiency measurement. It should be pointed out that although higher efficiency with higher output at high-line input, the efficiencies of 90- and 100-V output are almost the same at 90-V input, where it is critical to the thermal management. Furthermore, 100-V output for the output capacitor with 100-V voltage rating is not permitted in practice. With higher voltage rating capacitor, the cost increases. Therefore, the 90-V output is the cost efficient selection. The output voltage also affects PF significantly at low line as shown in Fig. 18.

Fig. 19 shows the measured efficiencies at different line voltages. It should be noted that the low-line efficiency is higher than the high-line efficiency over the load range below 70%. The efficiency difference between the low line and high line is less than 1% over the load range above 50%, which is desirable for the thermal optimization.
V. Conclusion

This paper has presented a detailed analysis and design considerations for COT controlled CRM buck PFC converter. It is shown that with an optimal design of output voltage and buck inductance, high efficiency and low-input harmonics of the circuit can be achieved. Experimental results obtained on a 100-W, 90-V output, and universal input prototype are given. The input current harmonics meet the IEC61000-3-2 standard with a large margin and the efficiency at full load maintains higher than 96.5% during the entire line voltage range. Although the discontinuous input current for Buck converter and variable switching frequency may result in larger filter, the high efficiency in universal-line range is still attractive for low-power ac–dc application.

References

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